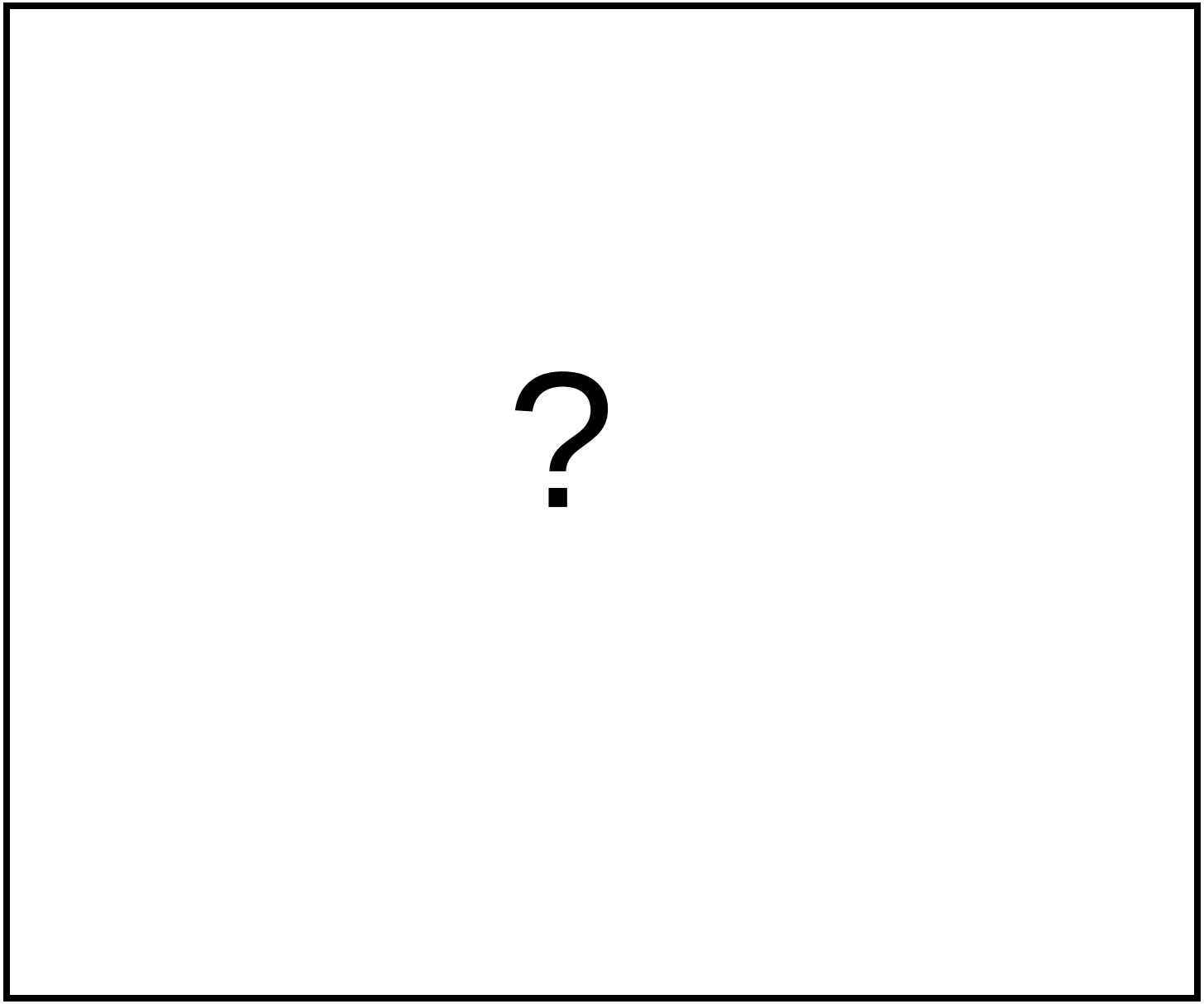
Course: Introduction to MONSOON

Ricardo Schmidt

La Serena 1-Jun-10

MONSOON



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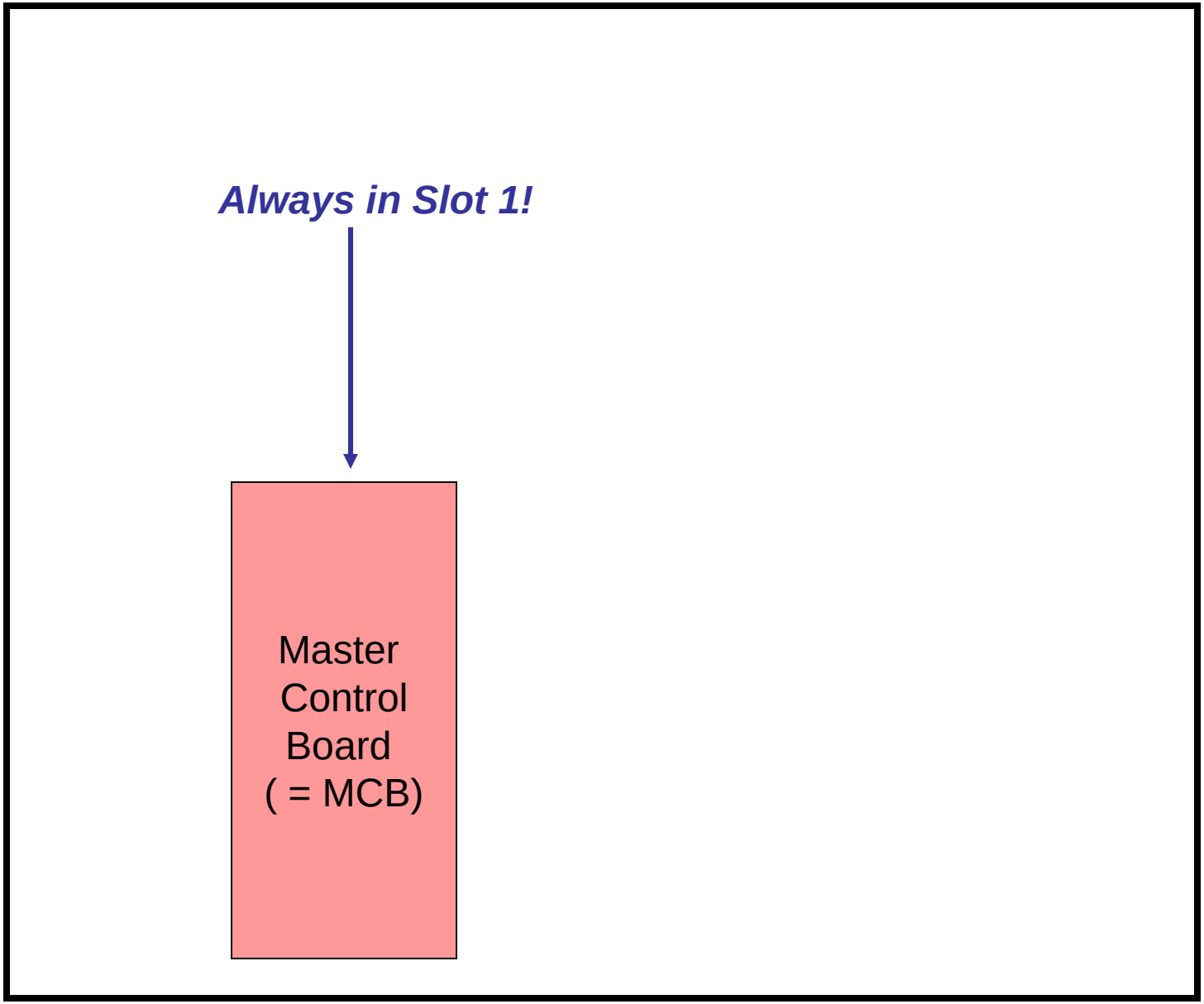

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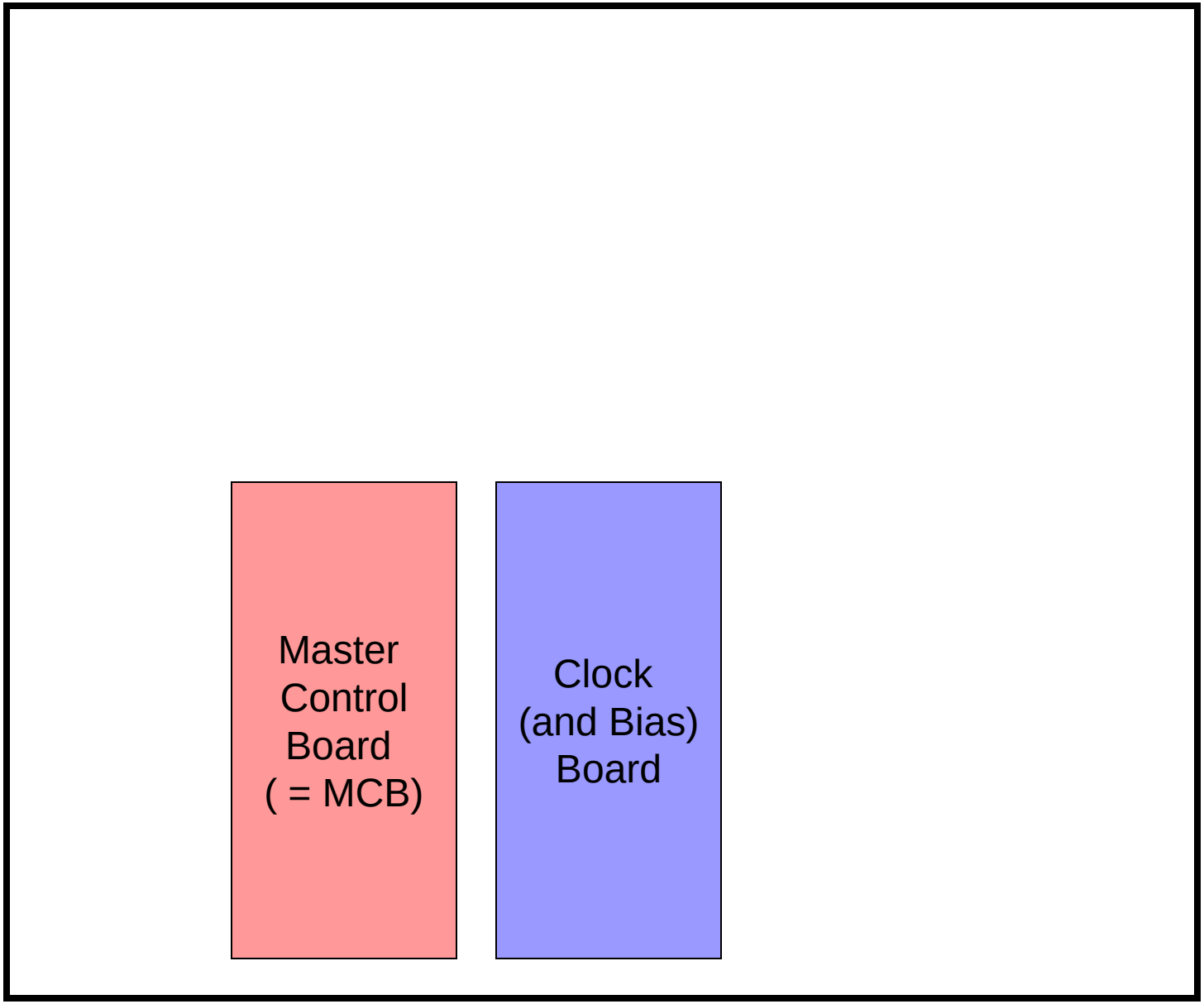

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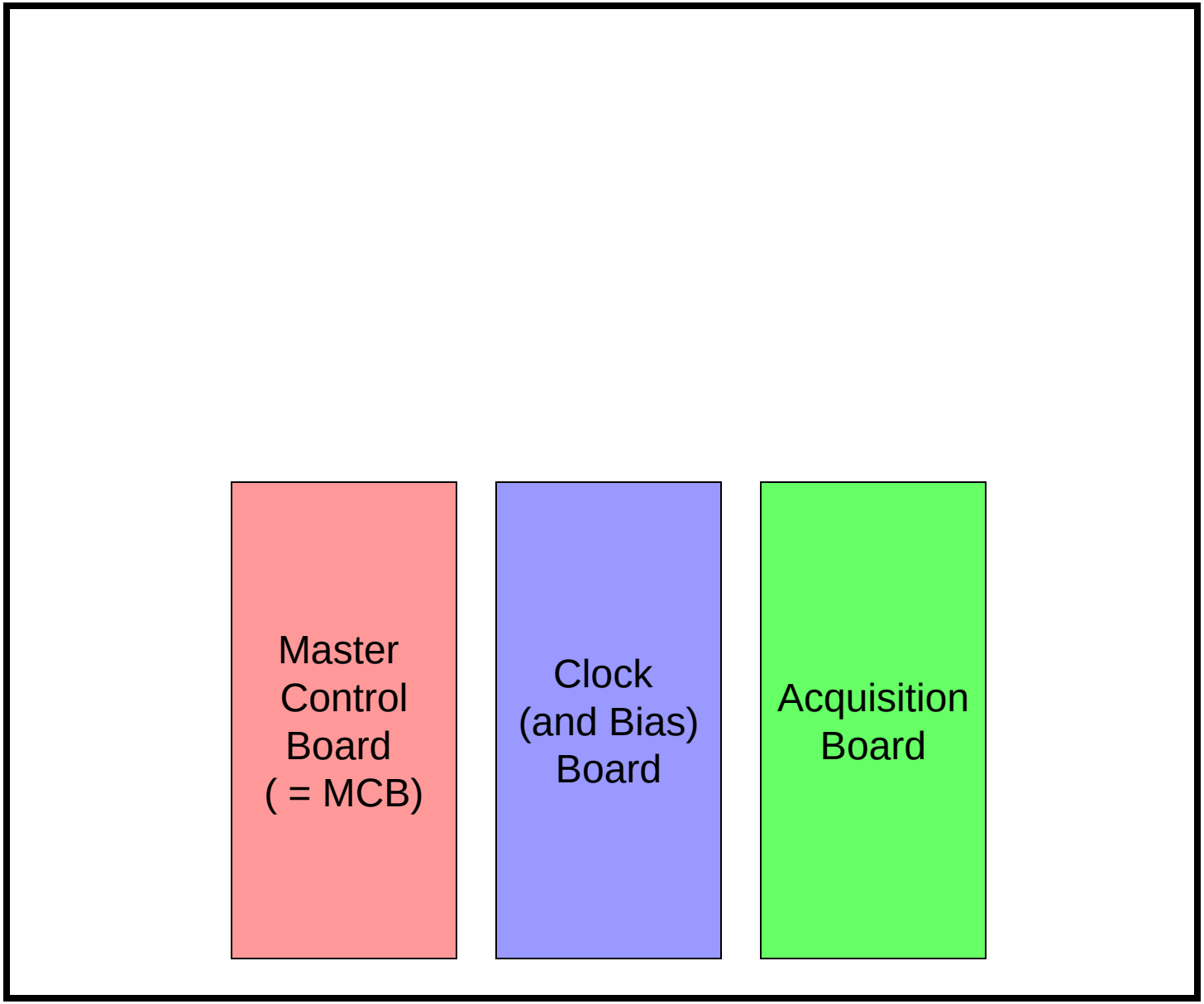
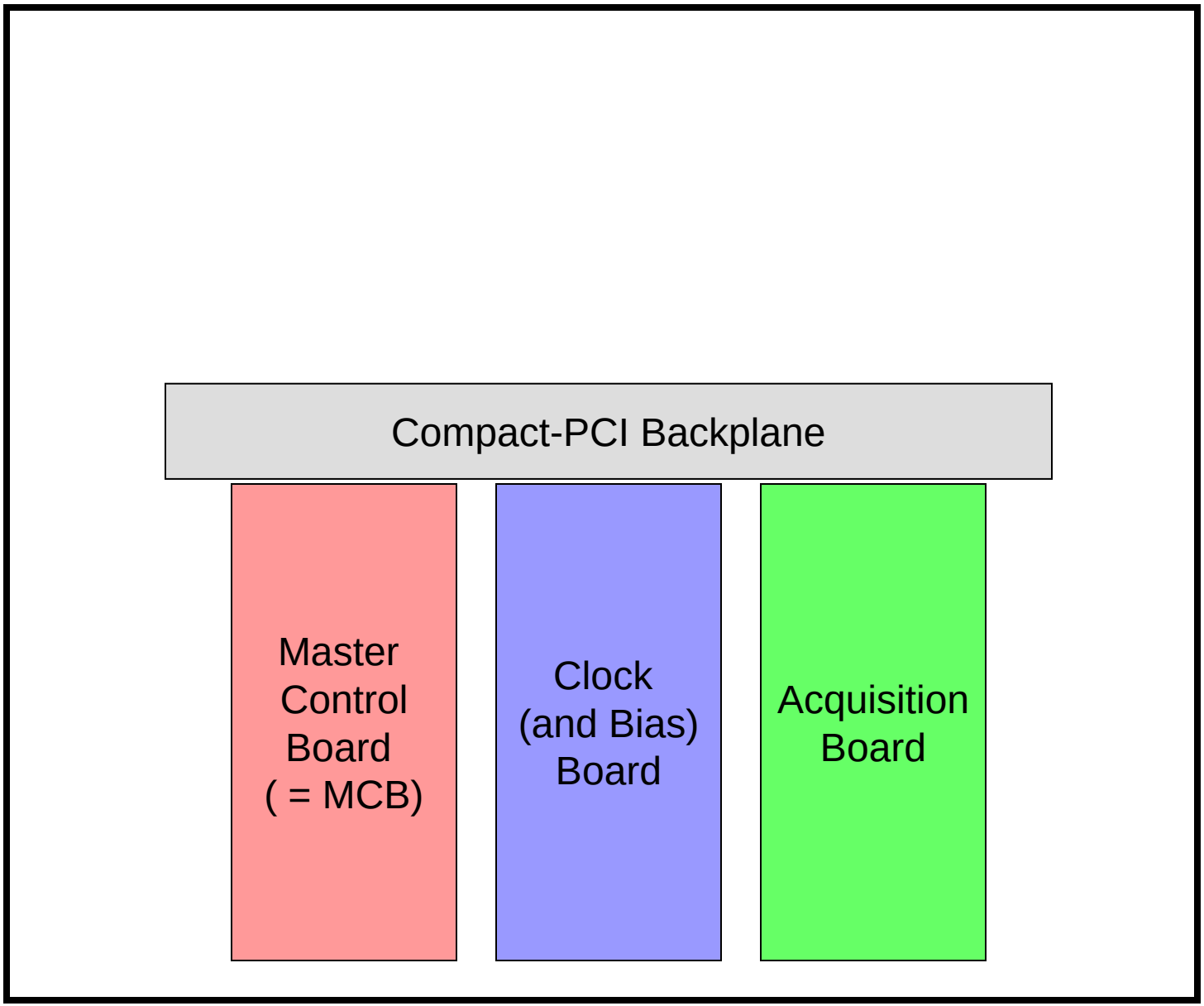
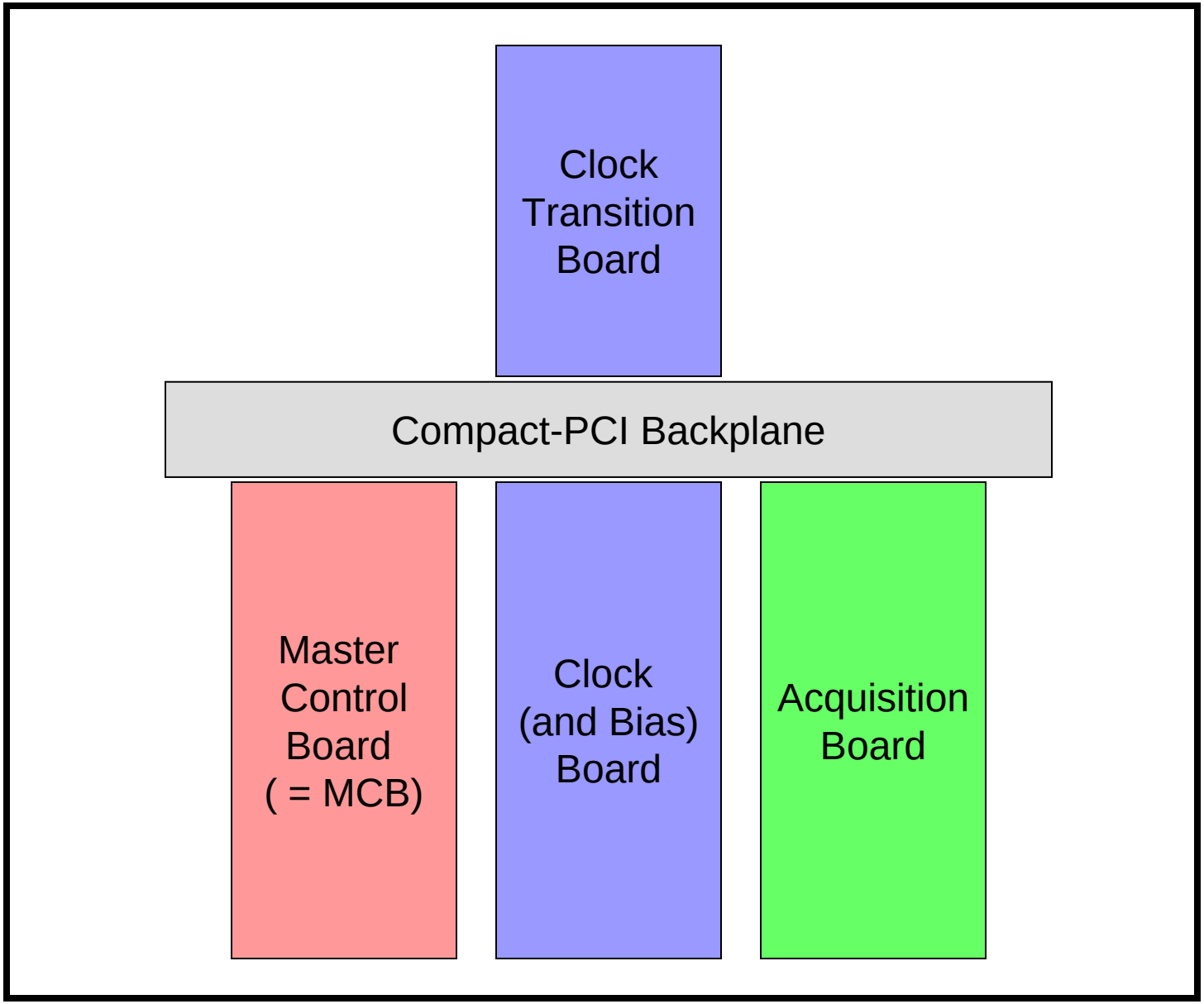

Master
Control
Board
(= MCB)
Clock
(and Bias)
Board
Acquisition
Board

MONSOON


Compact-PCI Backplane
Master Control Board (= MCB)
Clock (and Bias) Board
Acquisition Board

MONSOON


Clock
Transition
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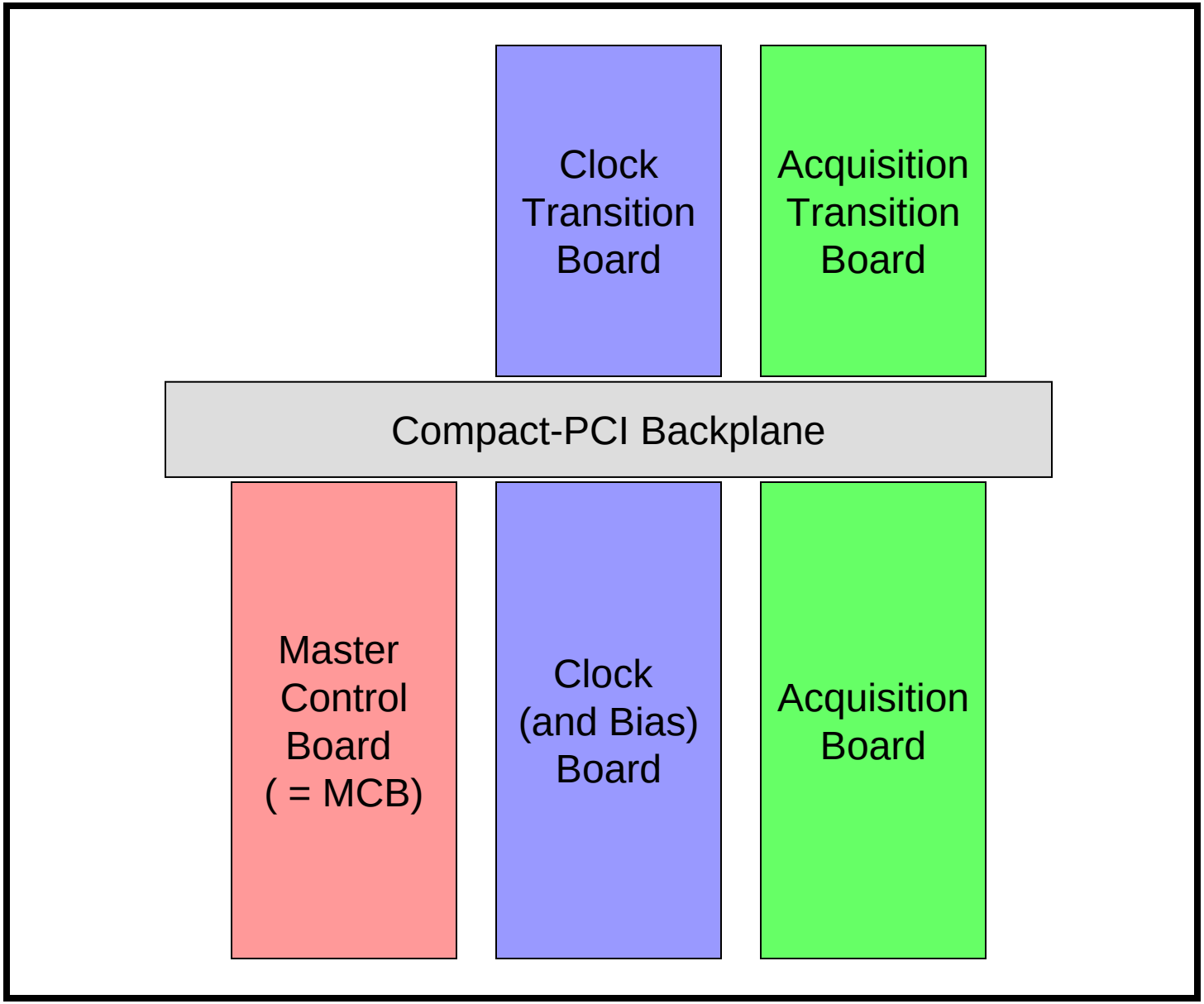
Clock Transition Board
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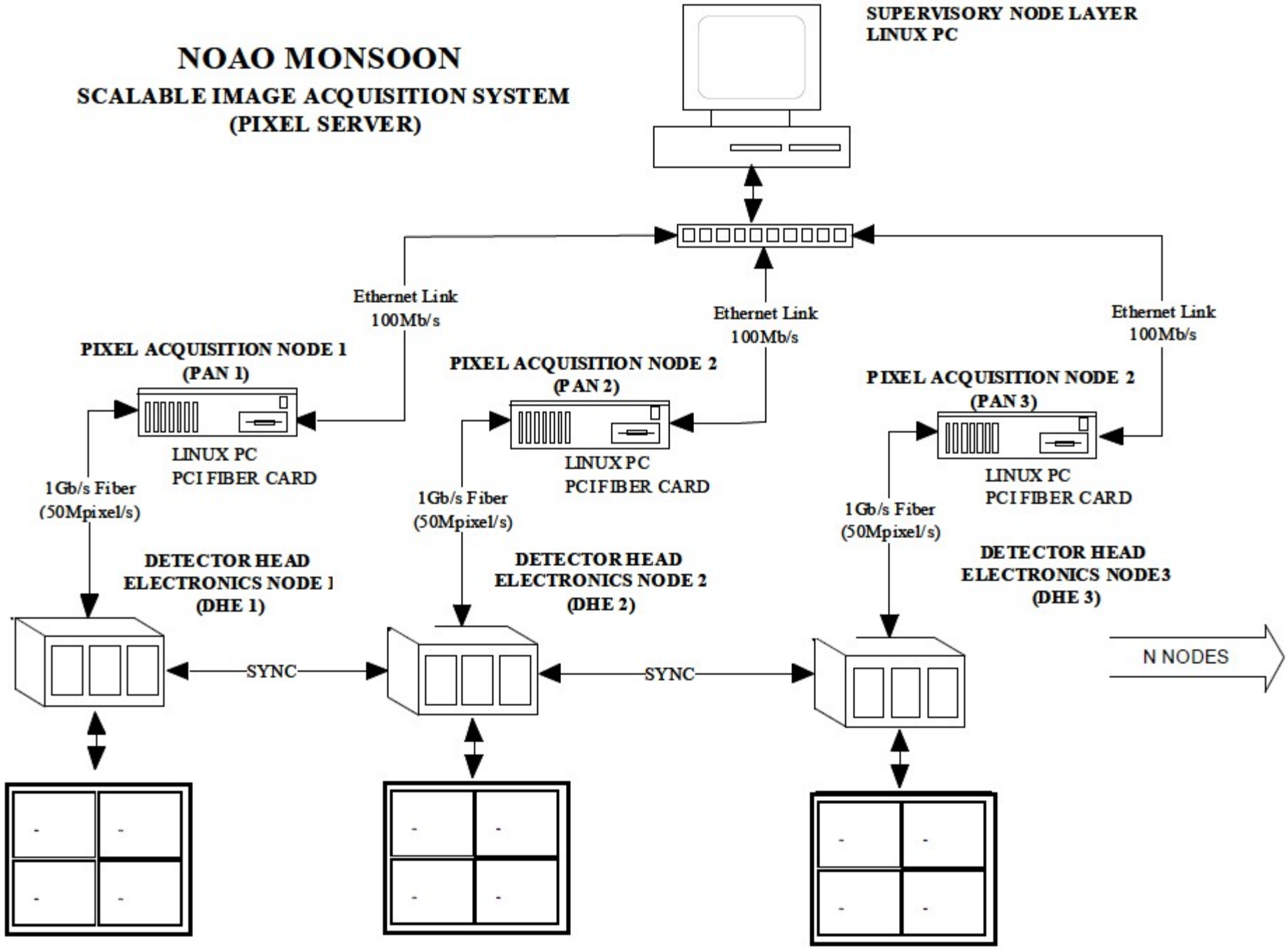
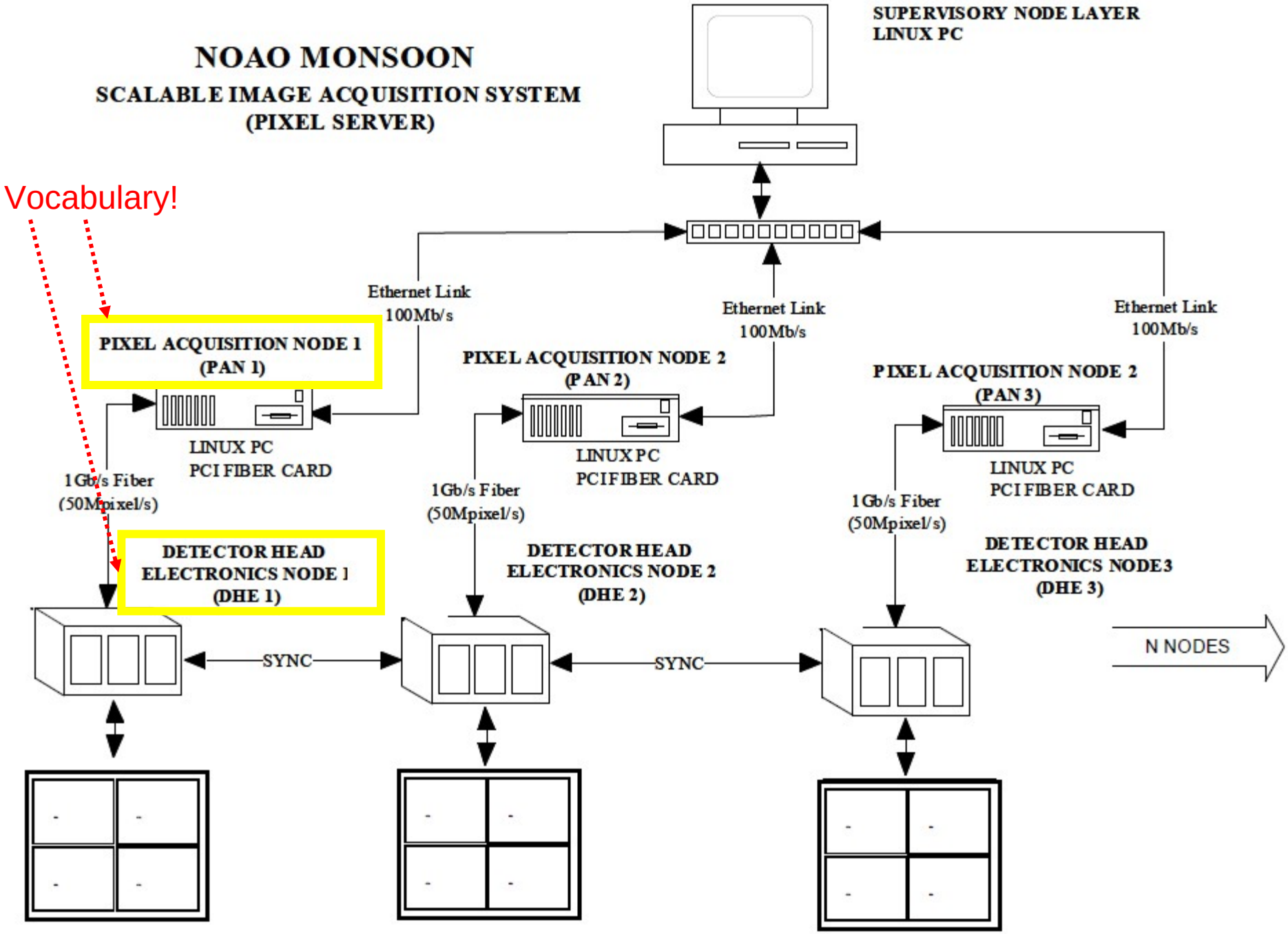
Acquisition Board

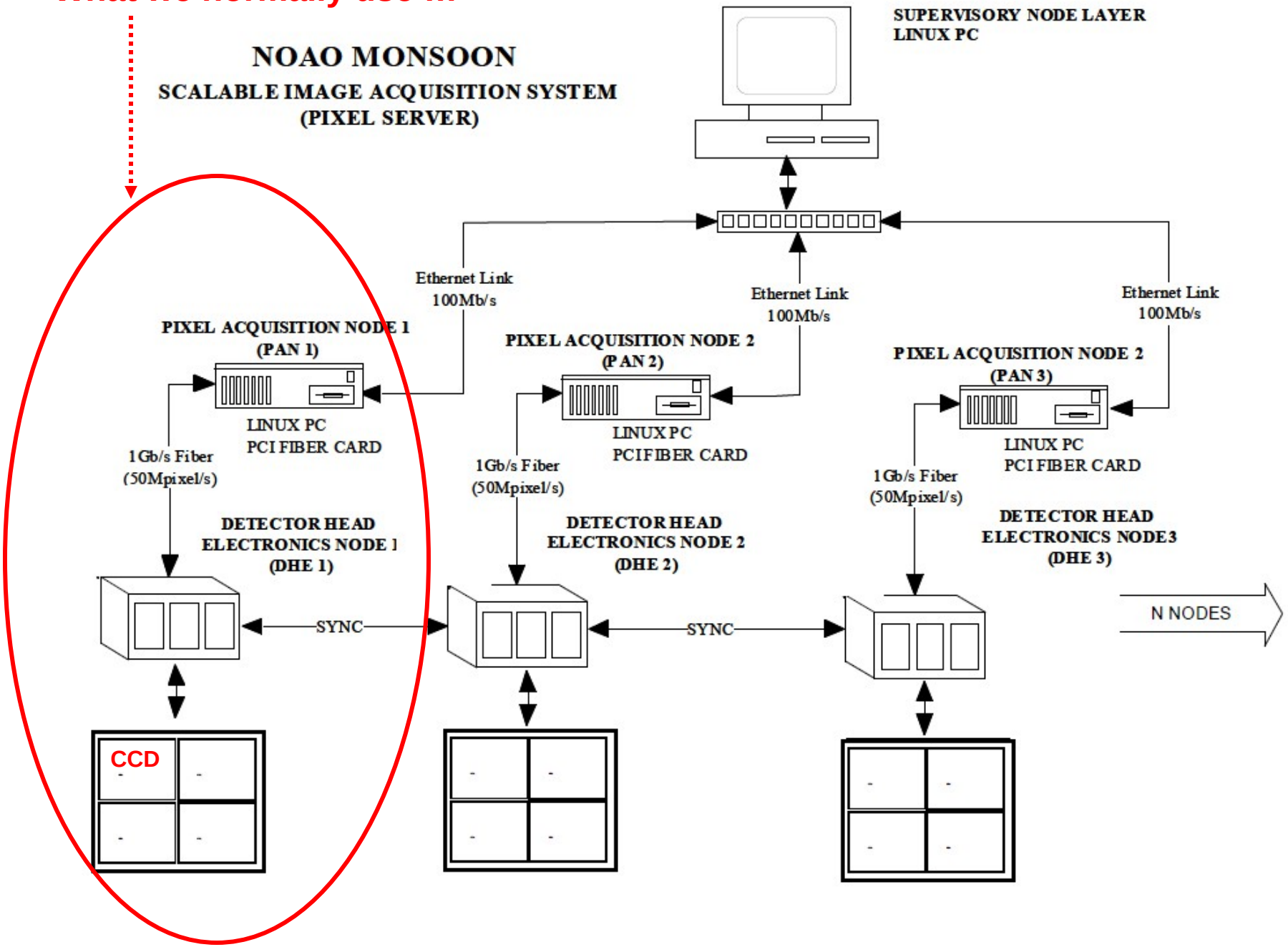
NOAO MONSOON

SCALABLE IMAGE ACQUISITION SYSTEM (PIXEL SERVER)




NOAO MONSOON
SCALABLE IMAGE ACQUISITION SYSTEM
(PIXEL SERVER)
SUPERVISORY NODE LAYER
LINUX PC
Vocabulary!
Ethernet Link
100Mb/s
Ethernet Link
100Mb/s
Ethernet Link
100Mb/s
PIXEL ACQUISITION NODE 1
(PAN 1)
PIXEL ACQUISITION NODE 2
(PAN 2)
PIXEL ACQUISITION NODE 2
(PAN 3)
LINUX PC
PCI FIBER CARD
LINUX PC
PCI FIBER CARD
LINUX PC
PCI FIBER CARD
1Gb/s Fiber
(50Mpixel/s)
1Gb/s Fiber
(50Mpixel/s)
1Gb/s Fiber
(50Mpixel/s)
DETECTOR HEAD
ELECTRONICS NODE 1
(DHE 1)
DETECTOR HEAD
ELECTRONICS NODE 2
(DHE 2)
DETECTOR HEAD
ELECTRONICS NODE3
(DHE 3)
SYNC
SYNC
N NODES

What we normally use …



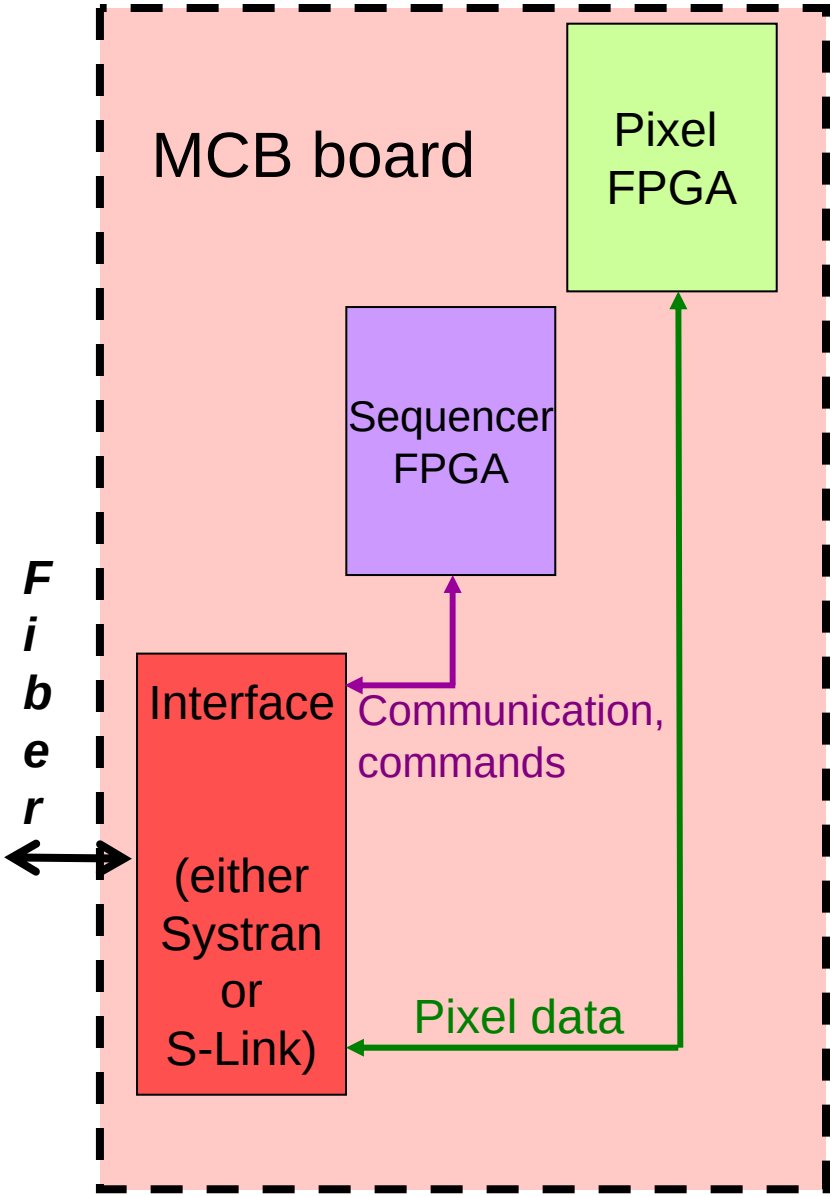
The Detector Head Electronics (= **DHE**, aka “the Monsoon controller”) typically comprises three types of boards:

-Master Control Board (= MCB),

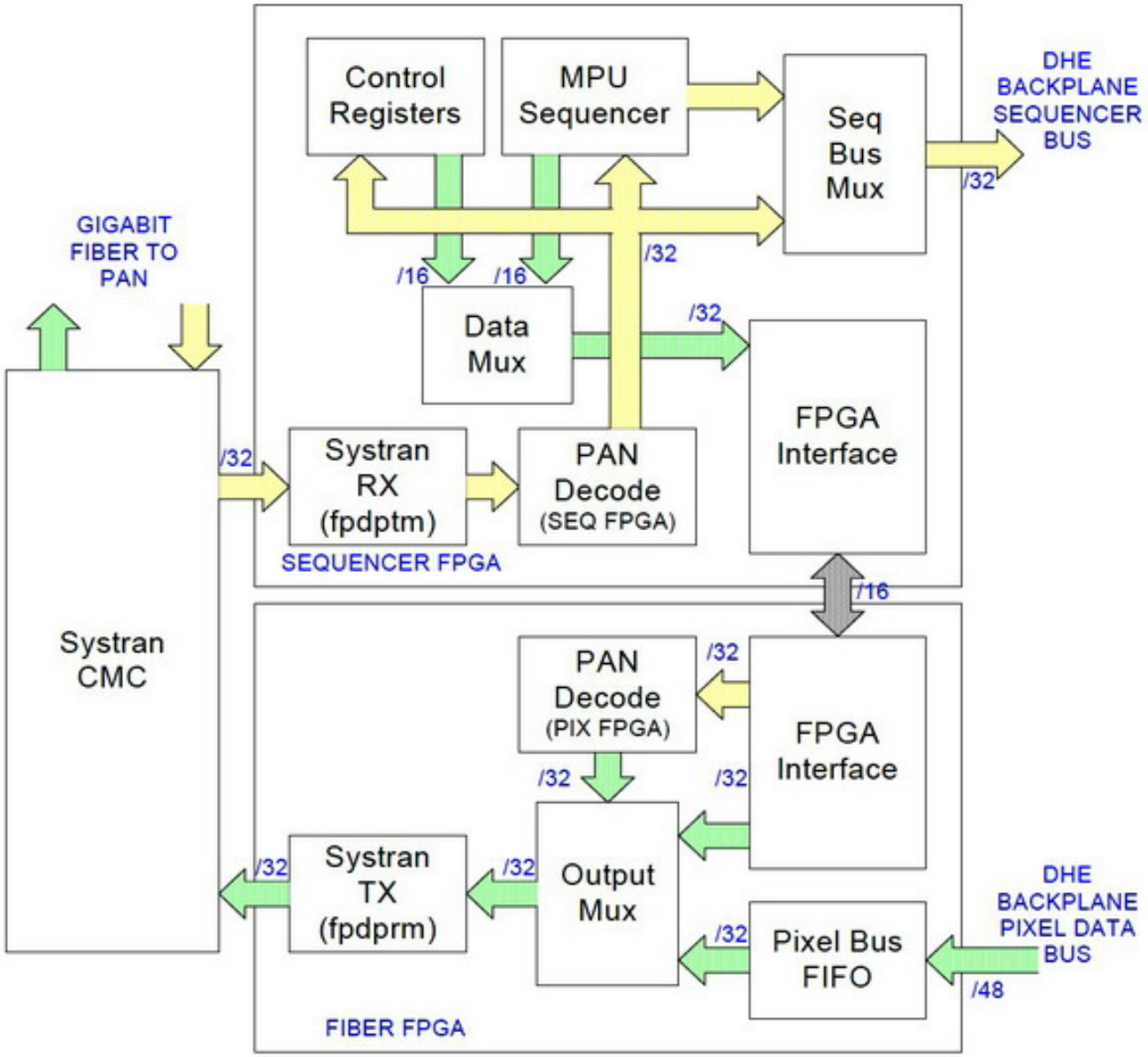
- Clock (and Bias) Board,

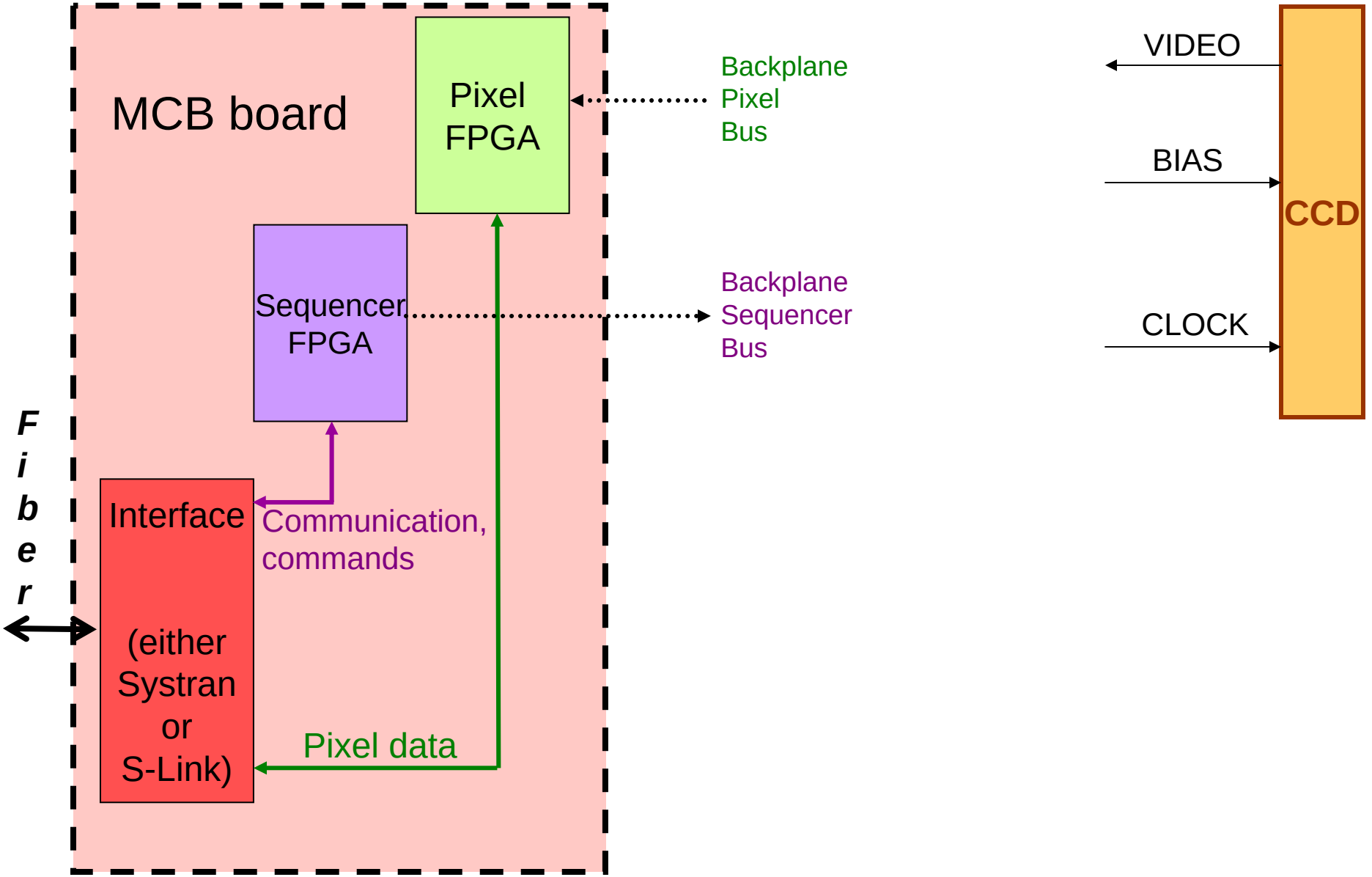
- Video Acquistion Board.

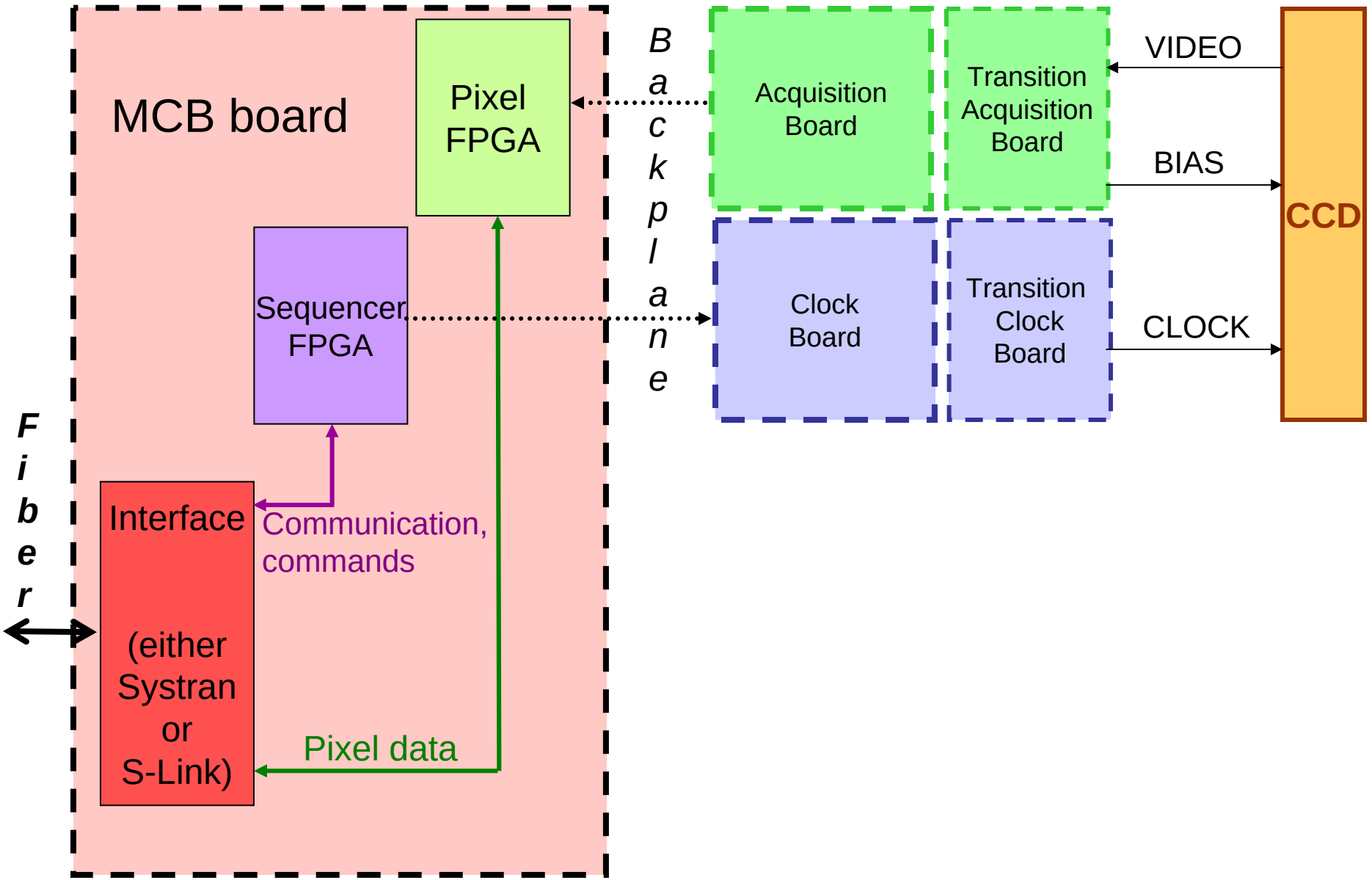
The current standard Configuration for the **DHE** is a 6U Eurocard format, using a standard 6U Compact PCI (= cPCI) backplane, for both the digital and analog interface, including the power distribution and interface to the focal plane. The digital part of the backplane follows cPCI signal integrity standards, but not the cPCI signal protocol in order to maximize system performance for the Monsoon applications.


MCB board
Pixel FPGA
Sequencer FPGA
Fiber
Interface
(either Systran or S-Link)
Communication, commands
Pixel data

MCB data paths




MCB board
Pixel FPGA
Backplane Pixel Bus
Sequencer FPGA
Backplane Sequencer Bus
Interface
(either Systran or S-Link)
Communication, commands
Pixel data
Fiber
VIDEO
BIAS
CLOCK
CCD


MCB board
Pixel FPGA
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Interface
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Communication, commands
Pixel data
Fiber
Backplane
Acquisition Board
Transition Acquisition Board
Clock Board
Transition Clock Board
VIDEO
BIAS
CLOCK
CCD

MONSOON

- Scalable to accommodate single or large mosaics of detectors.

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- Firmware source code is written in VHDL.
- A sequencer efficiently executes code that is downloaded to the MCB at system configuration time. The sequencer has the ability to control all hardware functions within the DHE i.e. clock and bias voltage levels, clock states, acquisition modes and timing, etc.

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- A small application is available to provide stand alone control over any MONSOON system. This application is called the MONSOON Engineering Console (MEC). As an alternative, Panview –developed in La Serena- can be used instead to control over Monsoon systems.

MONSOON

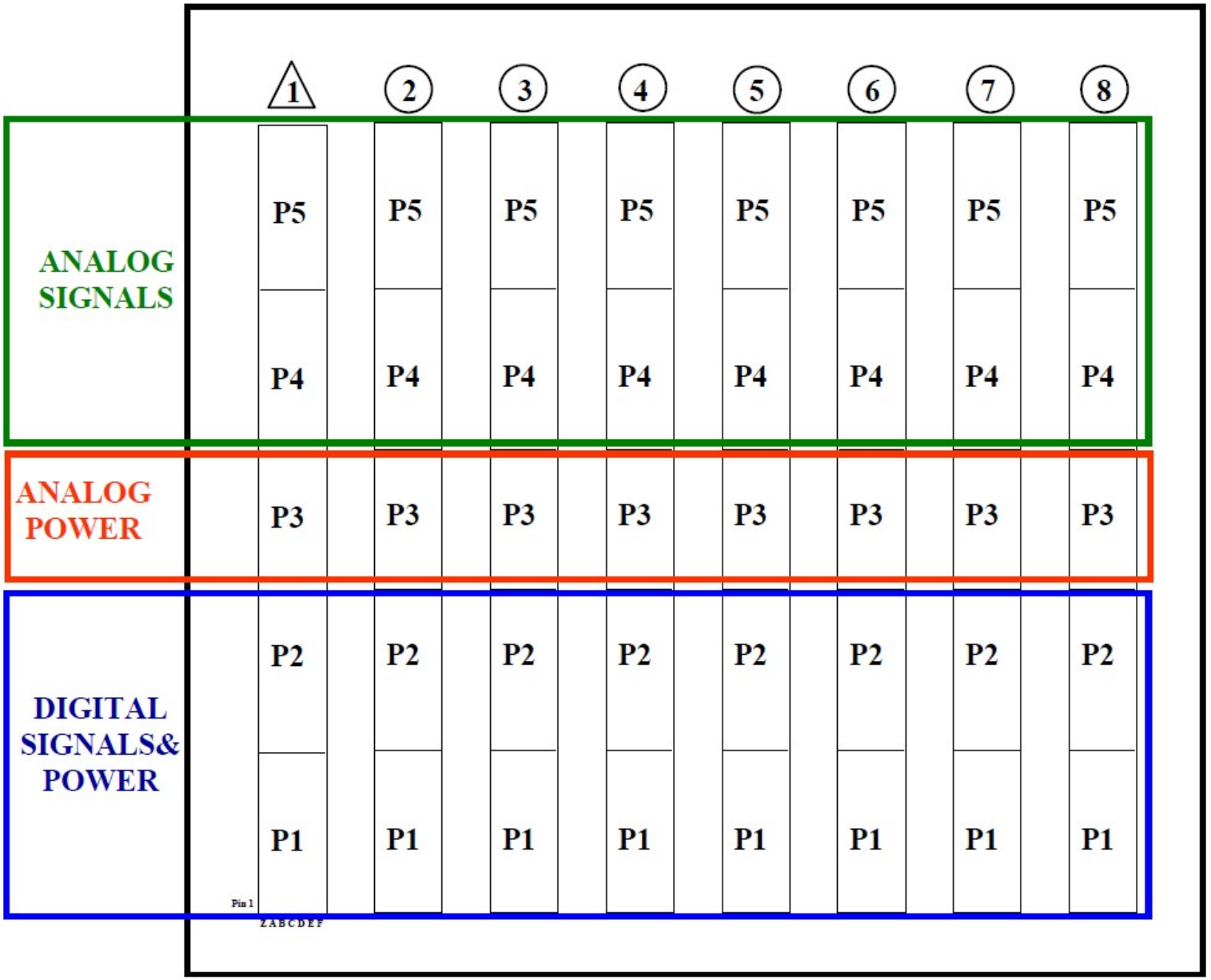
- **Monsoon on the web:**

http://www.noao.edu/ets/new_monsoon/

http://www.noao.edu/ets/new_monsoon/technical/general/

MONSOON cPCI Backplane Connectors

MNSN-AD-01-0006_ICD_7.0_V13.1.pdf



MONSOON

MNSN-AD-01-0006_ICD_7.0_V13.1.pdf

Backplane specifications.

The backplane is left justified, which means that the System Slot is to the left, with connector P1 at the bottom.

All connectors have 7 columns, named Z, A, B, C, D, E and F. All pins on columns Z and F are ground pins.

- P1 has 25 rows. Rows 12 to 14 are used as "keying area".
- P2 has 22 rows.
- P3 has 19 rows.
- P4 has 25 rows. Rows 12 to 14 are used as "keying area".
- P5 has 22 rows.

Front and rear connectors are **male** type. Maximum current per contact is 1.3 Amp (nominal at 50C).

MONSOON
MNSN-AD-01-0006_ICD_7.0_V13.1.pdf

Analog Power (P3/J3)

This connector provides the analog power and ground lines for the peripheral boards. The following voltages (and their respective returns) are defined on the connector:

- +5VA, -5VA, +/-5VA Return.
- +6.5VA, -6.5VA, +/- 6.5VA Return.
- +15VA, -15VA, +/-15VA Return.
- +16.5VA, -16.5VA, +/- 16.5VA Return.
- +HV1, -HV1, +/-HV1 Return (User-defined high voltage, normally used for detector drain bias.)
- +HV2, -HV2, +/-HV2 Return (User-defined high voltage, normally used for detector drain bias.)

It is not required that all the voltages be supplied or used on all the peripheral boards.

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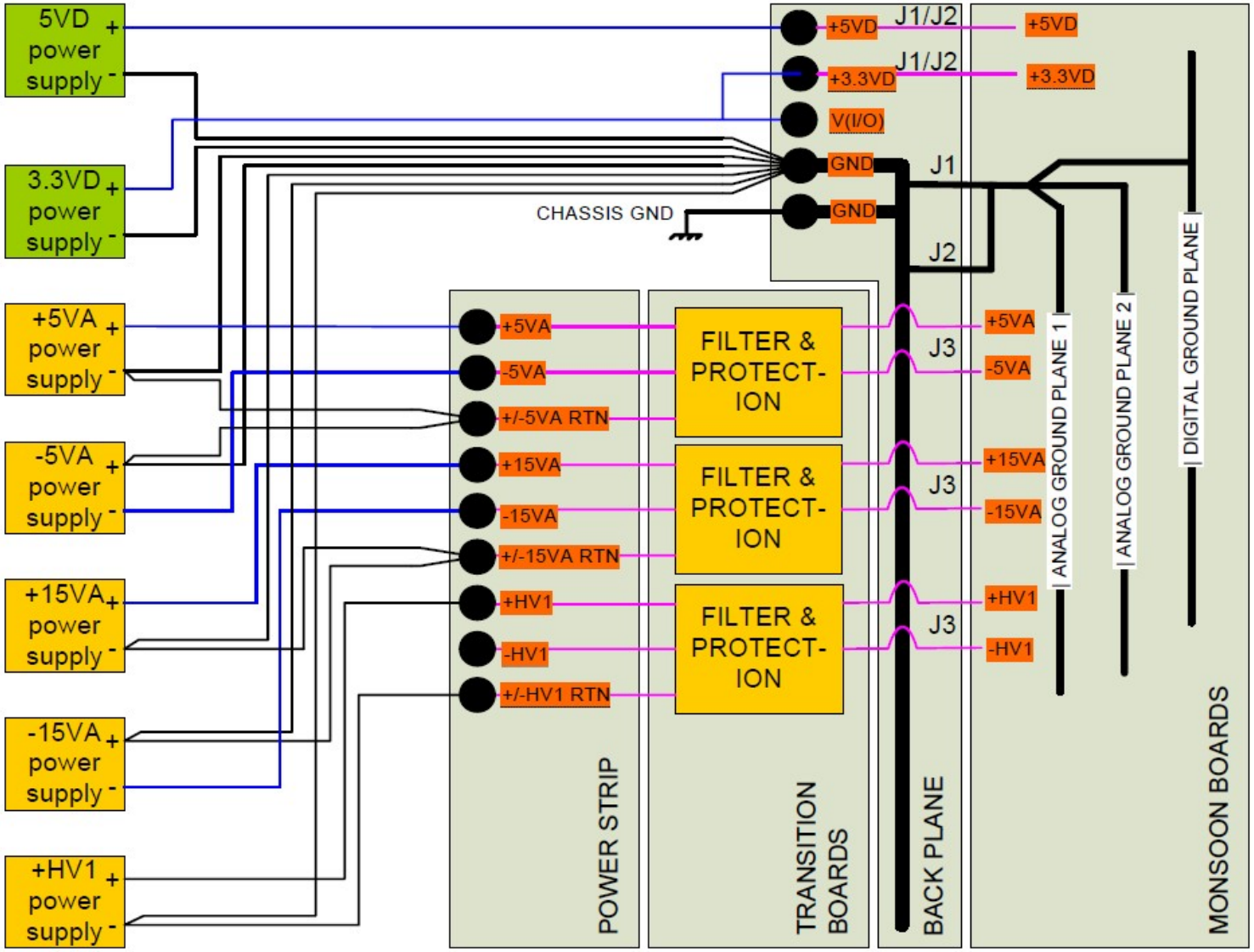
Connector J3/P3 (Analog Power)

Pin	A	B	C	D	E	F
19	+Vaux	+Vaux	+Vaux	+Vaux	+Vaux	AGND
18	-Vaux	-Vaux	-Vaux	-Vaux	-Vaux	AGND
17	+/-Vaux Return	+/-Vaux Return	+/-Vaux Return	+/-Vaux Return	+/-Vaux Return	AGND
16	+16.5VA	+16.5VA	+16.5VA	+16.5VA	+16.5VA	AGND
15	+/-16.5VA Return	+/-16.5VA Return	+/-16.5VA Return	+/-16.5VA Return	+/-16.5VA Return	AGND
14	-16.5VA	-16.5VA	-16.5VA	-16.5VA	-16.5VA	AGND
13	-6.5VA	-6.5VA	-6.5VA	-6.5VA	-6.5VA	AGND
12	+/-6.5VA Return	+/-6.5VA Return	+/-6.5VA Return	+/-6.5VA Return	+/-6.5VA Return	AGND
11	+6.5VA	+6.5VA	+6.5VA	+6.5VA	+6.5VA	AGND
10	Chassis GND	Chassis GND	Chassis GND	Chassis GND	Chassis GND	AGND
9	+5VA	+5VA	+5VA	+5VA	+5VA	AGND
8	+/-5VA Return	+/-5VA Return	+/-5VA Return	+/-5VA Return	+/-5VA Return	AGND
7	-5VA	-5VA	-5VA	-5VA	-5VA	AGND
6	-15VA	-15VA	-15VA	-15VA	-15VA	AGND
5	+/-15VA Return	+/-15VA Return	+/-15VA Return	+/-15VA Return	+/-15VA Return	AGND
4	+15VA	+15VA	+15VA	+15VA	+15VA	AGND
3	+/- HV Return	+/- HV Return	+/- HV Return	+/- HV Return	+/- HV Return	AGND
2	-HV	-HV	-HV	-HV	-HV	AGND
1	+HV	+HV	+HV	+HV	+HV	AGND

NOTES:

1. +/-Vaux is reserved for auxiliary power.
2. +/-HV is a user-defined high voltage power supply. Nominally +/-40V.

MONSOON



Typical Power Supply Connection Scheme

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Connector J5/P5 - CCD Acquisition (Video Inputs)

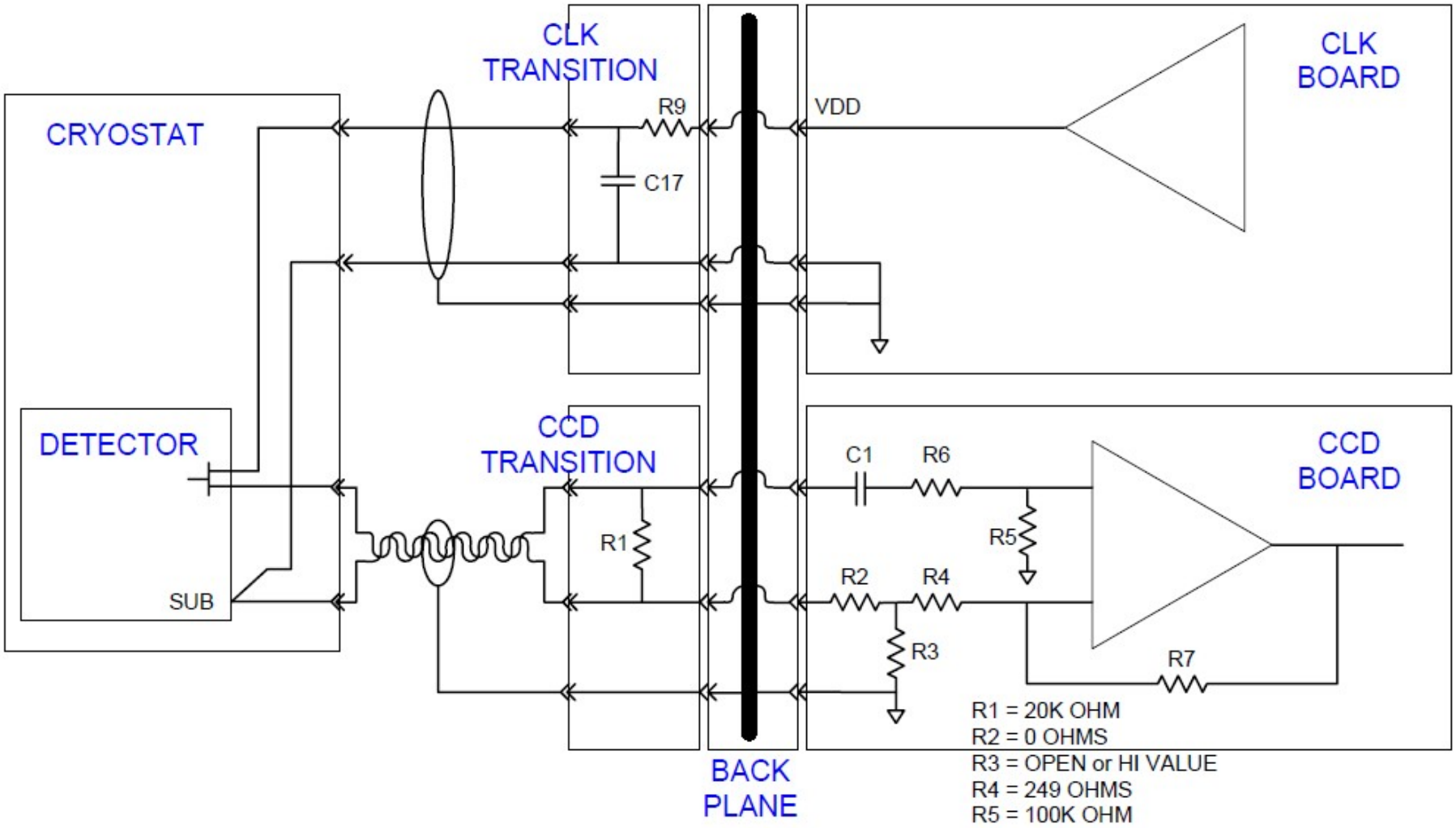
-

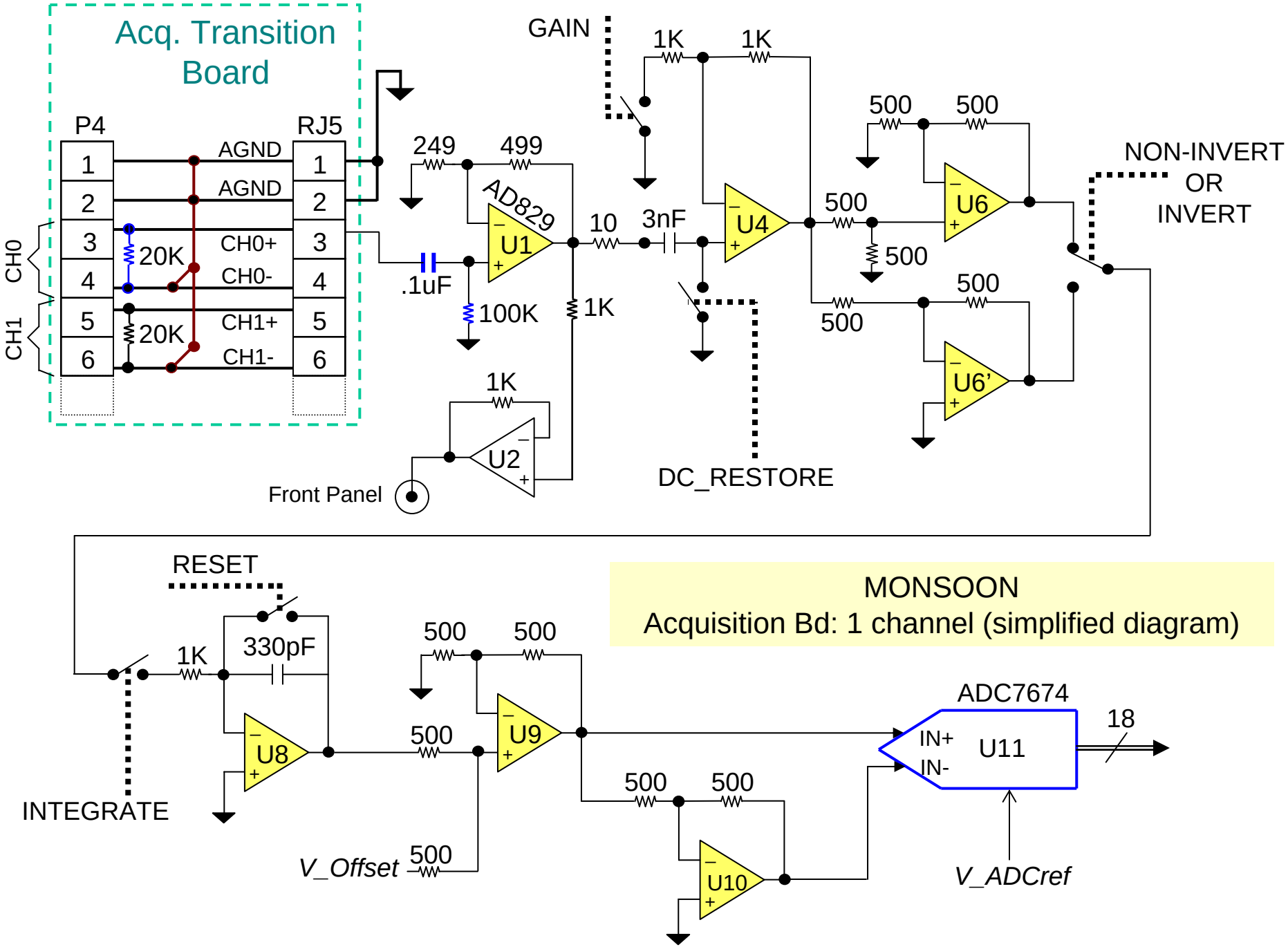
Pin	A	B	C	D	E	F
22			AGND			AGND
21			AGND			AGND
20	AGND	AGND	AGND	AGND	AGND	AGND
19	CH0-	CH0+	AGND			AGND
18	CH1-	CH1+	AGND			AGND
17	AGND	AGND	AGND	AGND	AGND	AGND
16			AGND			AGND
15			AGND			AGND
14	AGND	AGND	AGND	AGND	AGND	AGND
13	CH2-	CH2+	AGND			AGND
12	CH3-	CH3+	AGND			AGND
11			AGND			AGND
10			AGND			AGND
9	AGND	AGND	AGND	AGND	AGND	AGND
8	CH4-	CH4+	AGND			AGND
7	CH5-	CH5+	AGND			AGND
6	AGND	AGND	AGND	AGND	AGND	AGND
5			AGND			AGND
4			AGND			AGND
3	AGND	AGND	AGND	AGND	AGND	AGND
2	CH6-	CH6+	AGND			AGND
1	CH7-	CH7+	AGND			AGND

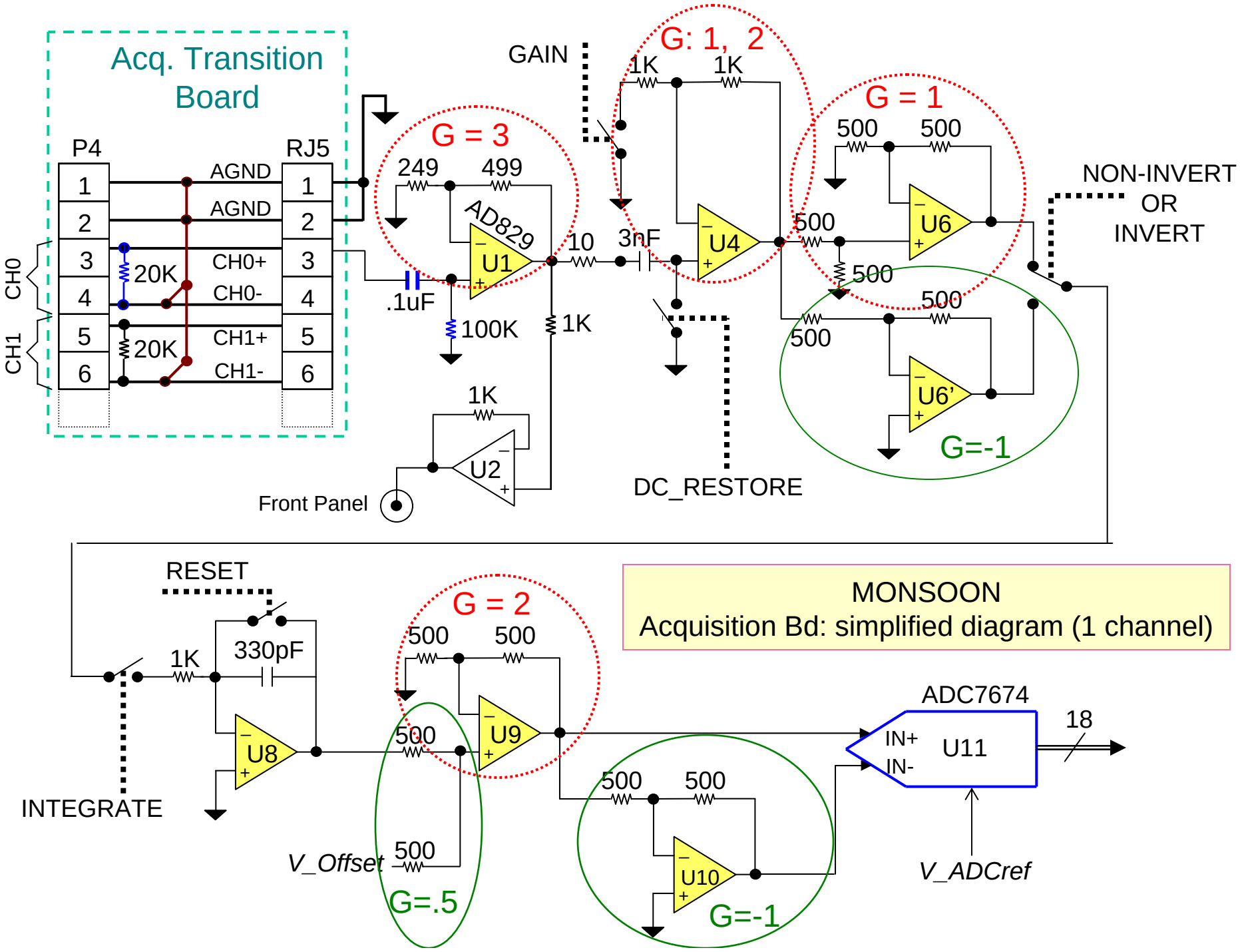
MONSOON

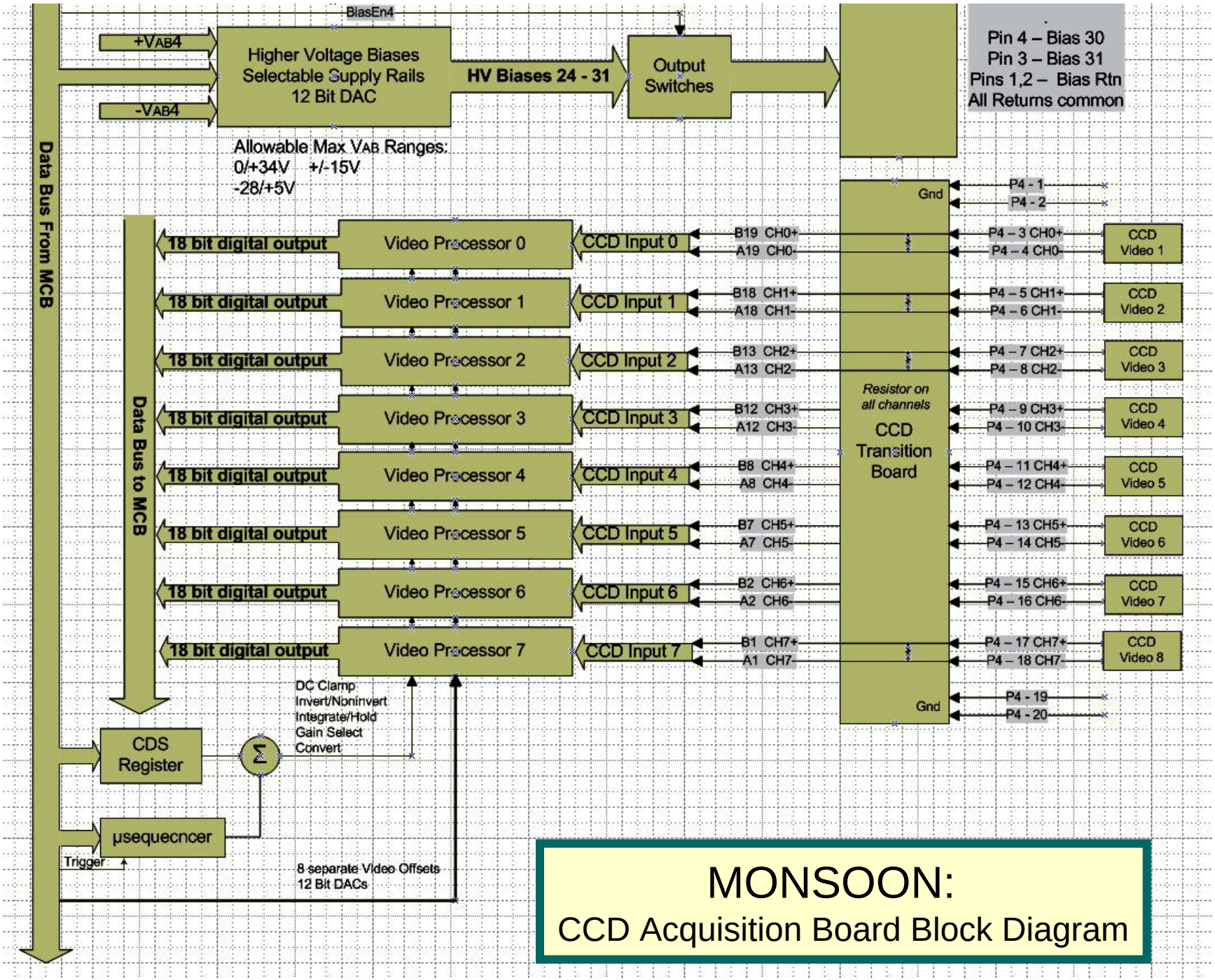
MNSN-AD-01-0006_ICD_7.0_V13.1.pdf

Typical Video Channel Connection Scheme




Acq. Transition Board
P4
RJ5
AGND
AGND
CH0+
CH0-
CH1+
CH1-
CH0
CH1
20K
20K
GAIN
1K
1K
249
499
AD829
U1
.1uF
100K
10
3nF
1K
U4
500
500
500
500
500
500
U6
U6'
NON-INVERT
OR
INVERT
1K
U2
Front Panel
DC_RESTORE
RESET
1K
330pF
U8
INTEGRATE
500
500
500
U9
500
500
500
U10
V_Offset
ADC7674
IN+
IN-
U11
18
V_ADCref
MONSOON
Acquisition Bd: 1 channel (simplified diagram)

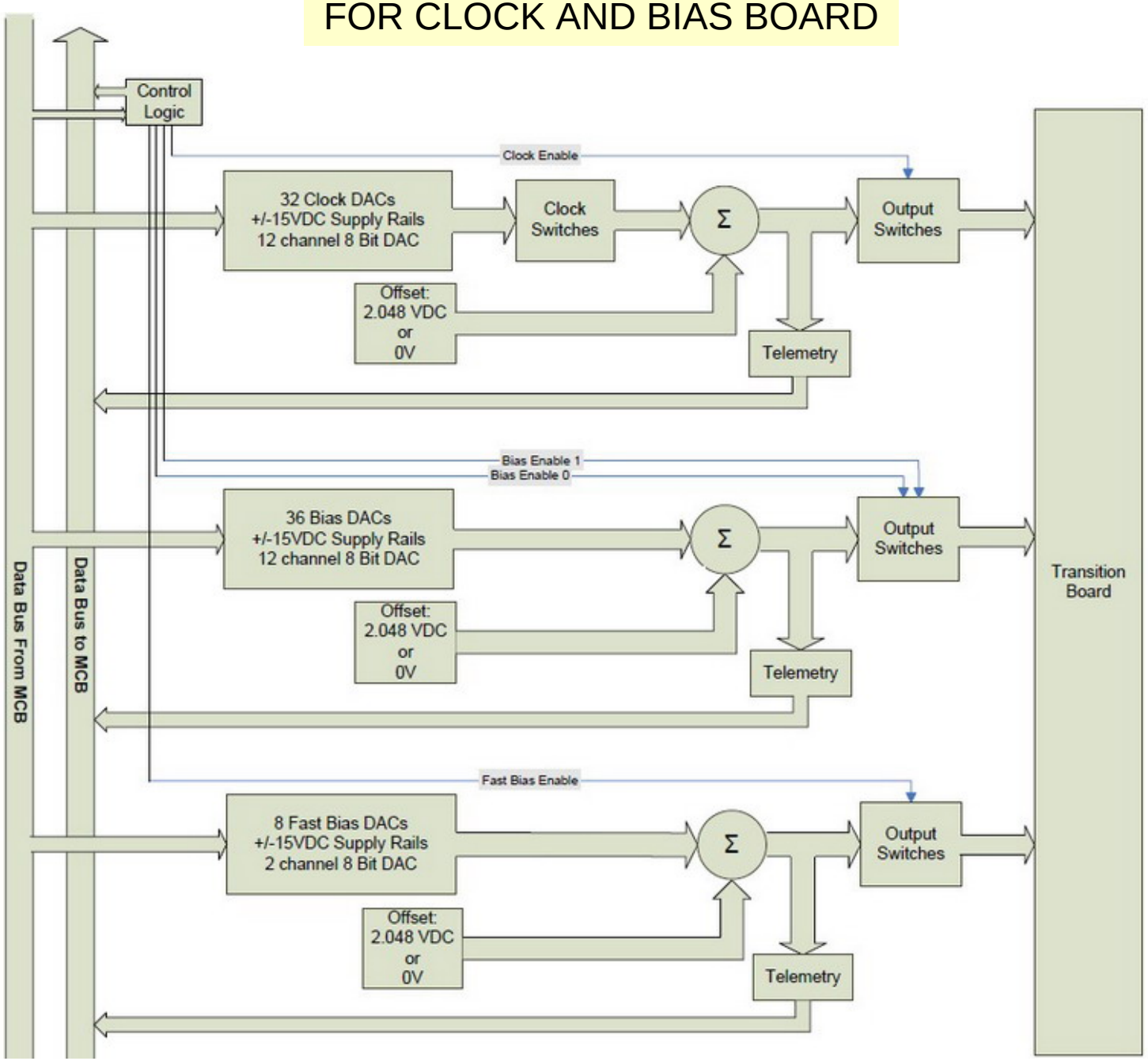

Acq. Transition Board
P4
RJ5
AGND
AGND
CH0+
CH0-
CH1+
CH1-
CH0
CH1
20K
20K
G = 3
249
499
AD829
U1
.1uF
100K
1K
10
3nF
GAIN
G: 1, 2
1K
1K
U4
G = 1
500
500
500
500
500
500
U6
U6'
G=-1
NON-INVERT OR INVERT
Front Panel
U2
1K
DC_RESTORE
RESET
1K
330pF
U8
INTEGRATE
G = 2
500
500
500
U9
V_Offset
500
G=.5
500
500
U10
G=-1
ADC7674
IN+
IN-
U11
18
V_ADCref
MONSOON
Acquisition Bd: simplified diagram (1 channel)



MONSOON:

CCD Acquisition Board Block Diagram

MONSOON: BLOCK DIAGRAM FOR CLOCK AND BIAS BOARD



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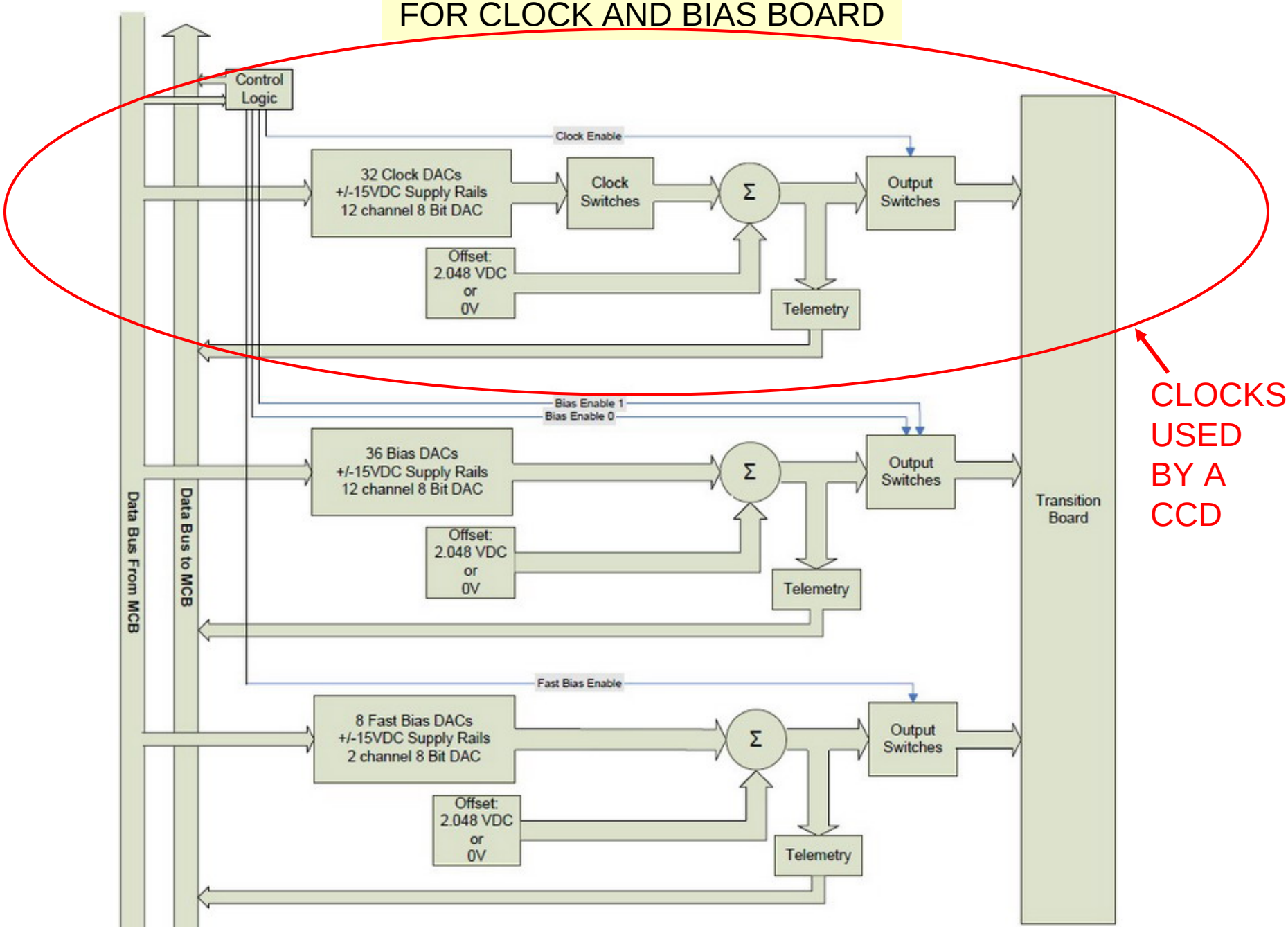
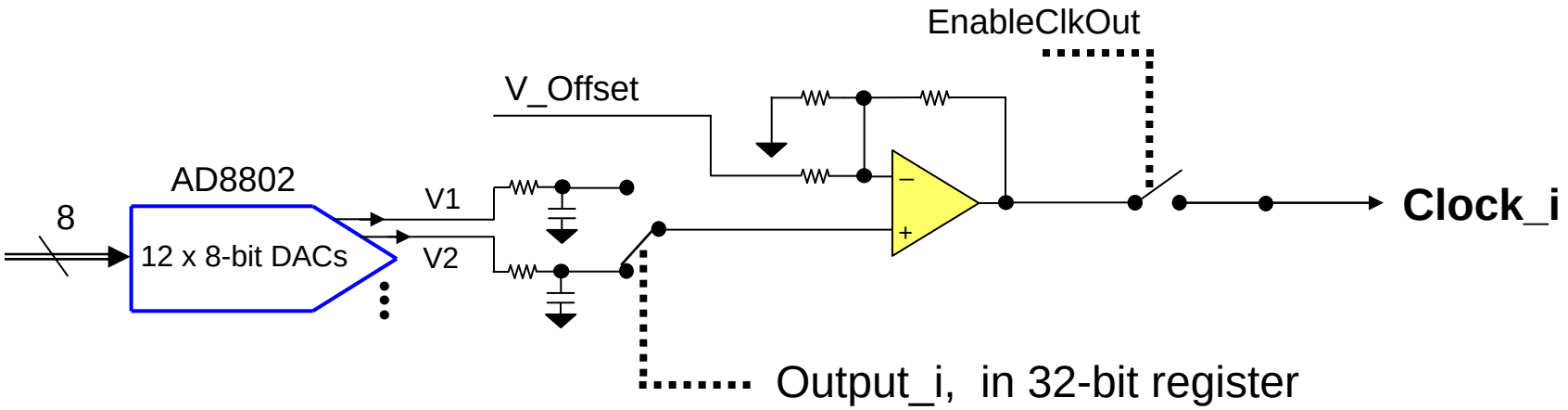


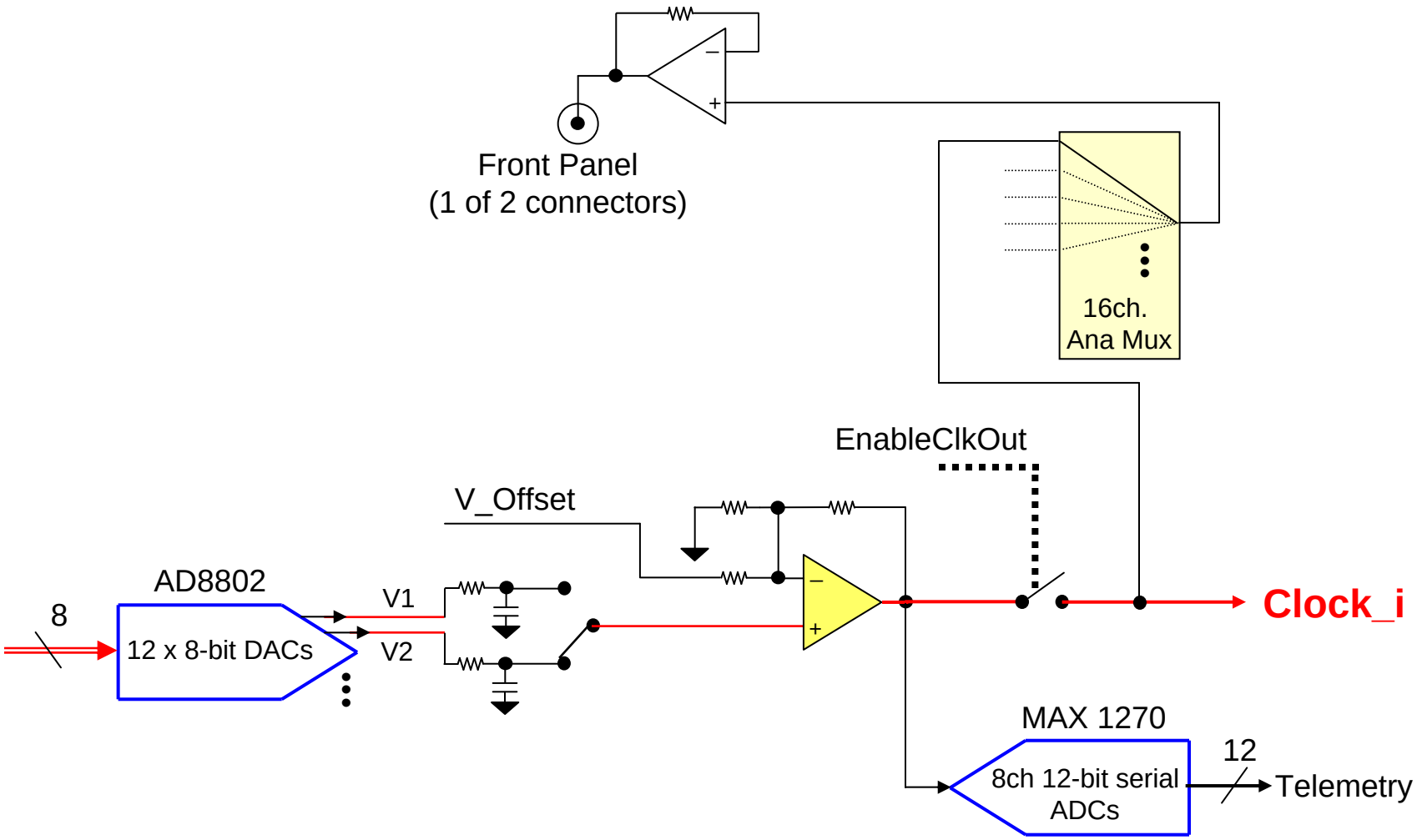
CLOCKS USED BY A CCD

MONSOON
Clock Bd: detail for Clock_i (1 out of 32)

Any clock: { *Vmax = +- 12.5V*
Imax = 30 mA



MONSOON
Clock Bd: simplified diagram for Clock_i (1 out of 32)



MONSOON

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Clock Lines through the Backplane

As mentioned above, there are independent clock lines going from the system slot to the peripheral slots. Every peripheral slot has its corresponding clock on the same pin (P1:D6). The peripheral boards use only this pin. Table 1 shows the distribution of the clocks to the different slots. Note that these current assignments reflect the 6-slot Schroff backplane (Designated as CPCI 2.0 R3.0) routing.

Table 1 - Clock Lines Distribution

System Slot			Peripheral Slot		
Pin Name	**Original CPCI Name**	**Pin Number**	**Logical Slot Number**	**Pin Name**	**Pin Number**
CLK2	CLK6	P2:A21	2	CLK	P1:D6
CLK3	CLK5	P2:A20	3	CLK	P1:D6
CLK4	CLK1	P2:A1	4	CLK	P1:D6
CLK5	CLK2	P2:A2	5	CLK	P1:D6
CLK6	CLK3	P2:B2	6	CLK	P1:D6
CLK7	CLK	P1:D6	?	CLK	P1:D6
CLK8	CLK4	P2:A3	?	CLK	P1:D6

•The DHE hardware modules are:

- Master Control Board – controls communication to the Pixel Acquisition Node (PAN) computer, DHE bus control and detector clock sequencing. An MCB is required for any DHE.

- Clock and Bias Board – generates low voltage biases and clock signals. A Clock and Bias Board is required for any DHE. NOTE: CBB version used by Newfirm is not compatible with CBB used by CCDs (component and grounding differences exist).

- IR Acquisition Board – acquires up to 36 channels of DC-coupled video signal. An IR Acquisition Board would be found in an IR type DHE only.

- CCD Acquisition Board – acquires up to eight channels of AC-coupled video signals and provides high voltage biases. A CCD Acquisition Board would be found in a CCD type DHE only.

DHE boards beyond MCB, CBB and CAB:

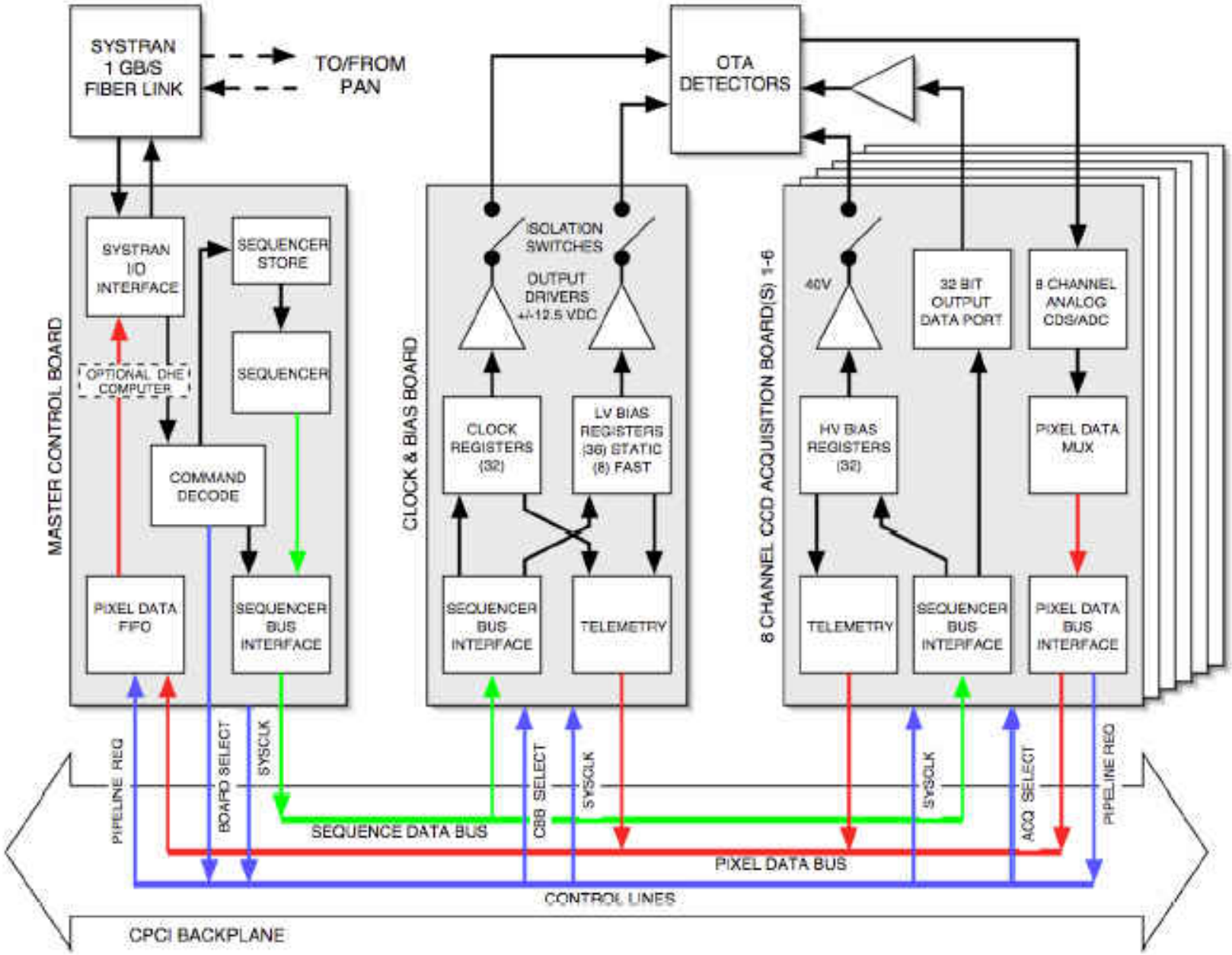
Additionally, there are Transition Boards within the DHE for the Clock and Bias Board, the IR Acquisition Board and the CCD Acquisition Board. The purpose of the Transition Board is threefold:

- The transition board provides the interface from the appropriate DHE primary module to the detector inputs or outputs, e.g., the CCD Acquisition Transition Board interfaces the output(s) of a CCD to the CCD Acquisition Board.

- The second purpose of the Transition Board is to provide a means of routing the analog voltages for the DHE modules to the respective DHE modules.

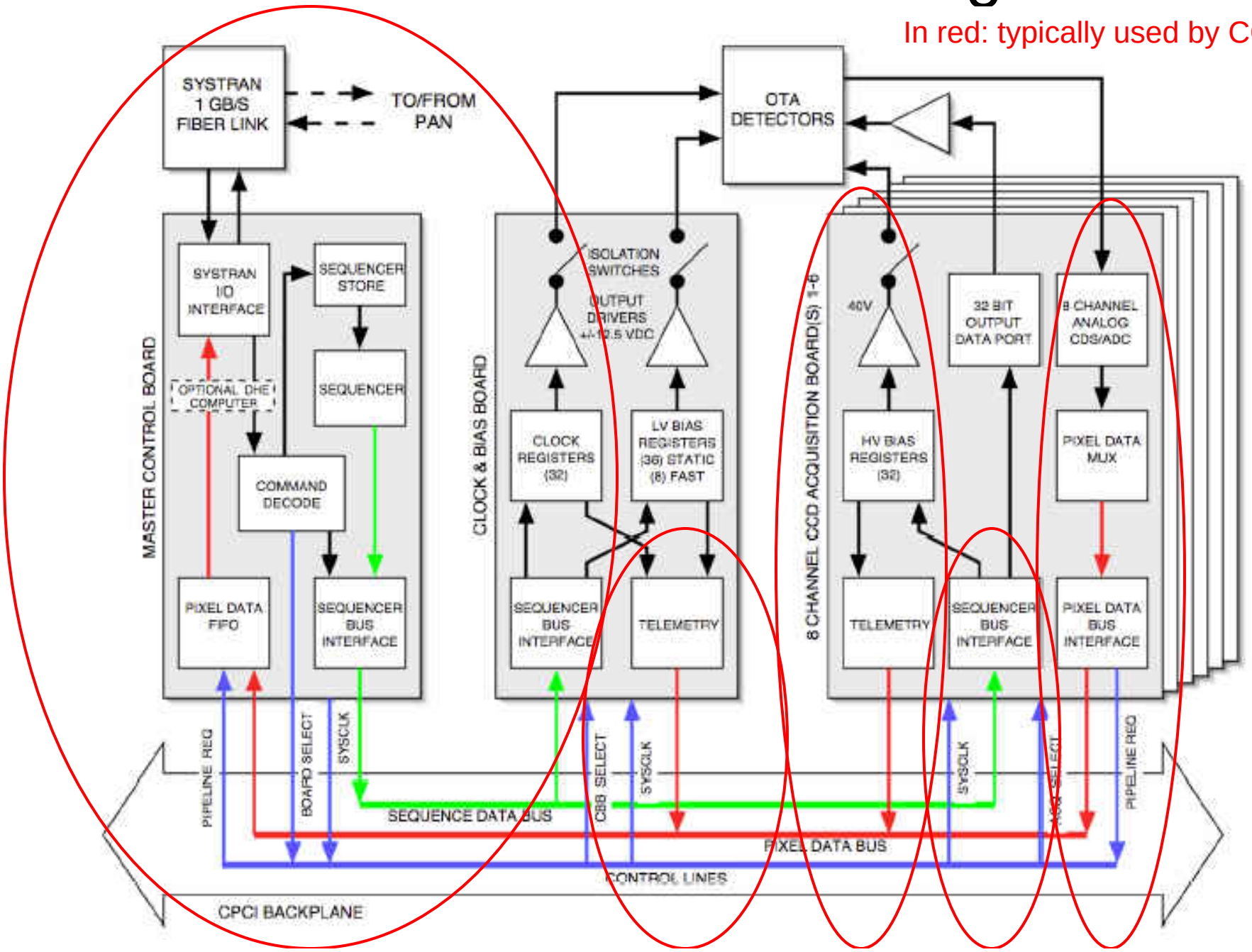
- The acquisition transition boards (CCD and IR) provide device protection circuitry.

NOAO Monsoon Block Diagram

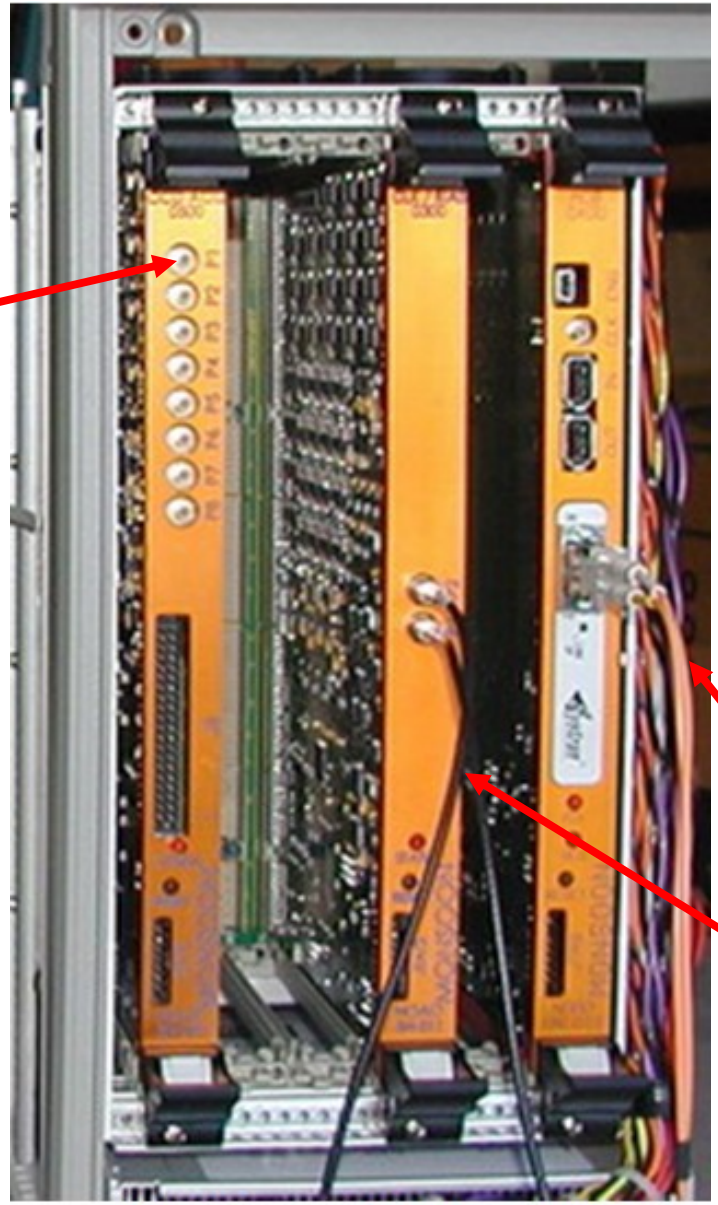


NOAO Monsoon Block Diagram

In red: typically used by CCD



MONSOON


“Video” monitoring points
Fibers
Coaxes to oscilloscope
Boards:
CAB
CBB
MCB

MONSOON

What MONSOON circuit boards are required to run a CCD?

Three. They are:

- 1 Master Control Board (MCB)
- 1 Clock & Bias) Board (CBB)
- 1 eight-channel CCD Acquisition Board (CAB) (= "video" board).

The minimum requirement is 1 MCB + 1 CBB + 1 CAB

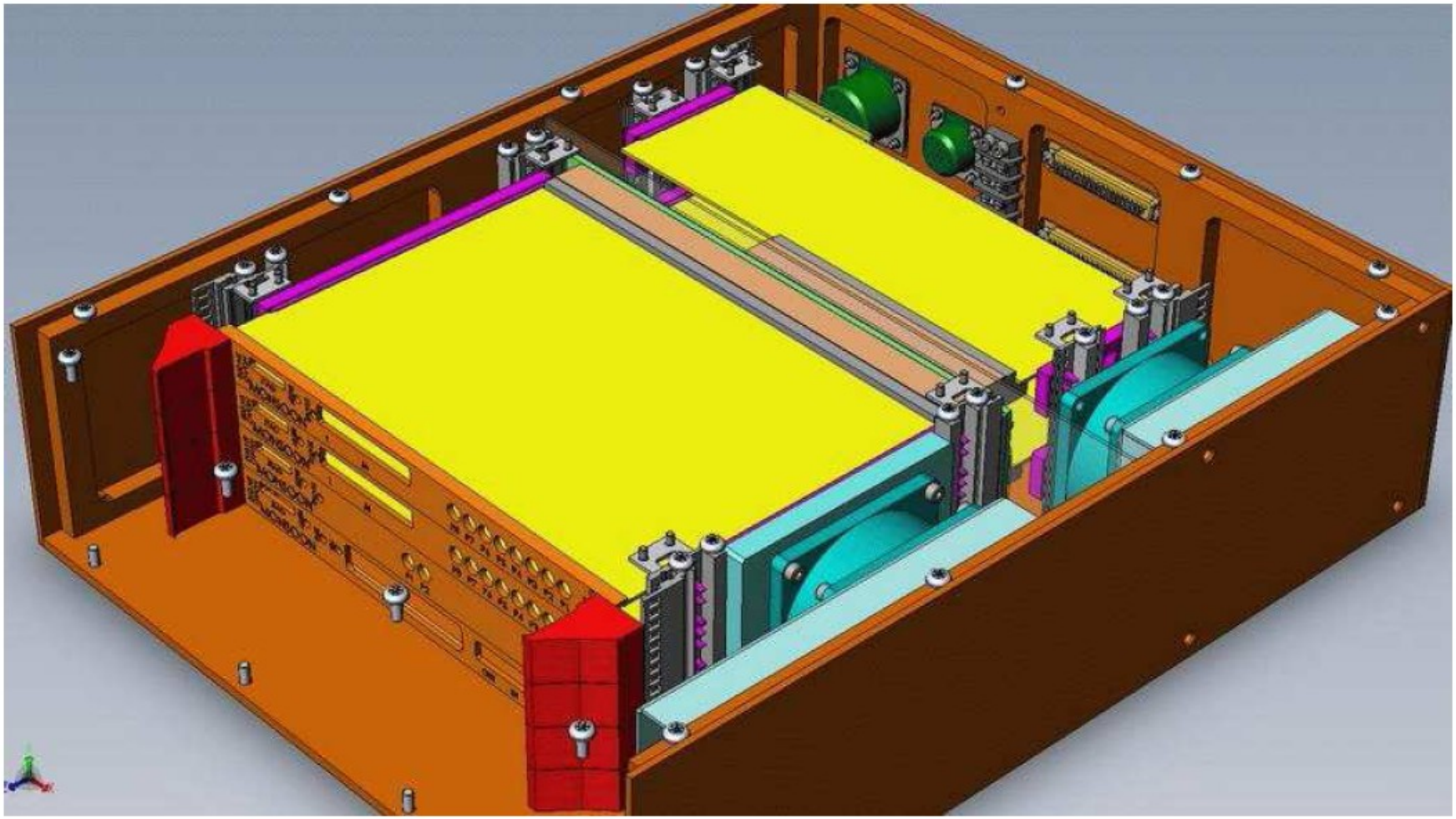
Can more than one of any type board run in one MONSOON chassis?

MCB = No, only 1 per crate.
CBB = Yes
CAB = Yes

In simple terms, what are the functions of the MCB, CBB and CAB boards?

- MCB controls CBB and CAB and interfaces to the PAN computer.
- The CBB supplies the CCD clocks.
- CAB supplies the CCD biases and receives the video input signal generated by the CCD.

MONSOON



Monsoon Orange conceptual drawing. Box size 435x390x108 mm, mass 9.9 kg.

MONSOON

Are the CBB and CCDACQ board connected directly to the detector?
No, each of these boards has a corresponding interface (or “transition”) board that is located inside the MONSOON chassis right behind the board. These interface boards contain the connectors that receive the cables running between the MONSOON and the detector dewar. The MCB has no interface board.

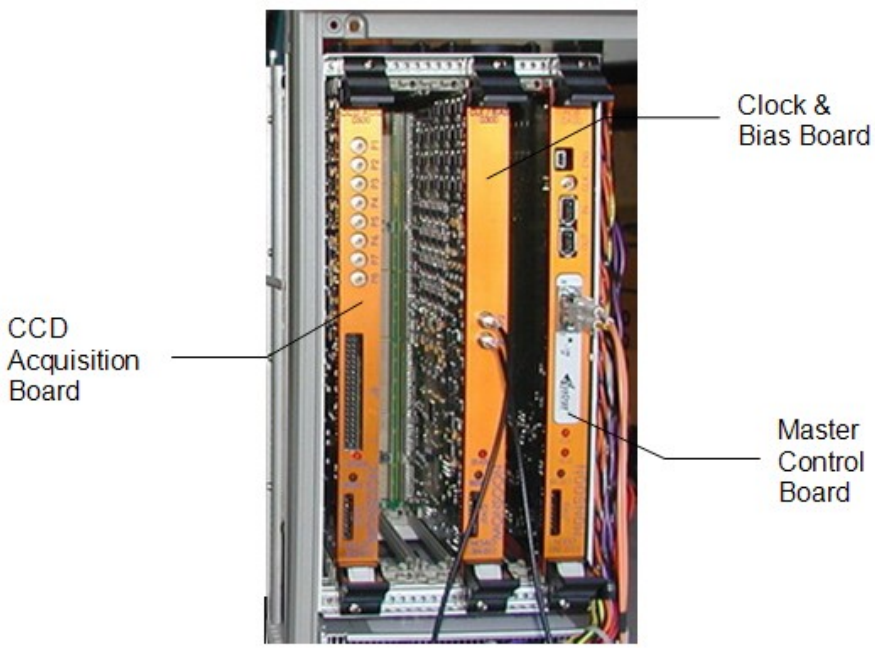
How many slots does a typical MONSOON chassis have?
Six slots. But Orange Monsoon (e.g.at the 60” telescope) uses a 4 slot chassis.

Is there a special slot for the MCB in a Monsoon crate?
Yes. It is Slot 1, next to one of the two lateral walls and identified by red colored card guides (it also may have a special marking such as a triangle).

How do slot numbers translate into slot addresses (as used by the MONSOON low level software to identify the location of each board in the MONSOON chassis)?
Slot 1 = address 1
Slot 2 = address 2
Slot 3 = address 4
Slot 4 = address 8
Slot 5 = address 16 (hex 10)
Slot 6 = address 32 (hex 20)

What actual adresses do get used in a real 6-slot lab system?

MCB = slot 1 (address 1)
CBB = slot 3 (address 4)
CAB = slot 6 (address 32)



Can clock waveforms be monitored with an oscilloscope?

Yes. There are two SMB connectors, P1 and P2, conveniently supplied on the front panel of the CBB. A buffered version of any of the clocks can be multiplexed toward P1 and / or P2.

Can the CBB bias section be powered off since it is not used by a CCD?

Yes. To turn off power to the bias section of the CBB:

1. Remove wires across L2 and L6. Refer to page 17 of schematics.
2. Remove jumpers JP1, JP2 and JP3. Refer to page 3 of schematics.

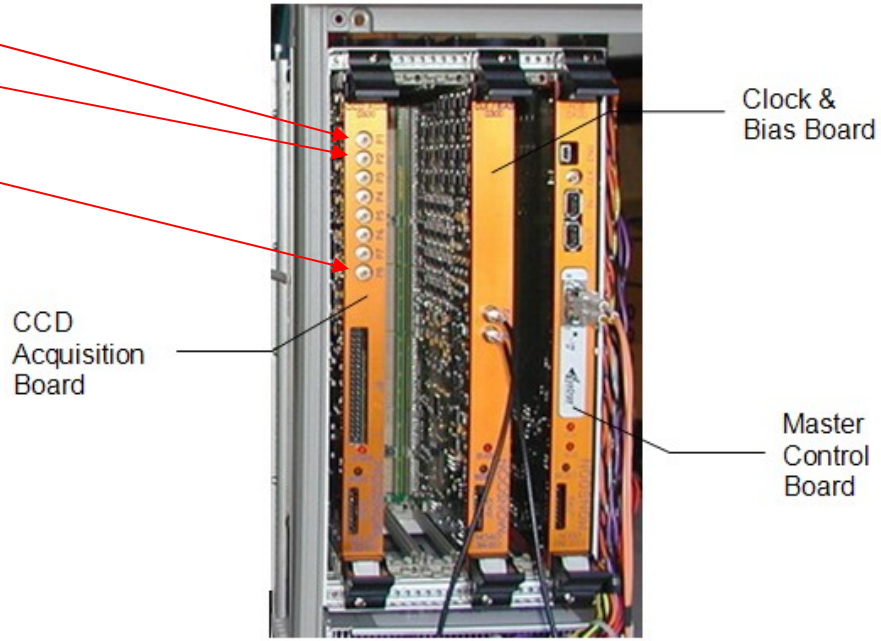
Can the CCD output signal be observed with an oscilloscope?

There are 8 SMB connectors, one per channel, located on the CAB front panel. A buffered copy of the CCD output signal -after it passes the AC coupling capacitor and gets (nominally) amplified by 3 in the first OpAmp- is available at the respective XXX connector. Note that connectors and channels are matched in the following manner:

- P1 corresponds to channel 0
- P2 corresponds to channel 1

and so forth through

- P8 which corresponds to channel 7



MONSOON

Can the video signal processor control signals be checked with an oscilloscope?
Yes, but it is less straightforward than observing the CCD output signals. Header J6 on the front panel has many of its pins pre-assigned so that a copy of these digital control signals (Invert [INV], NonInvert [NIN], DC_restore [DCR], Integrator_Reset [RST], Integrate [INT], ADC_start_convert [CTC], etc.) is made available according to Table 3 in document MNSN-AD-08-0004, Clock and Bias Board description. Be careful not to touch the adjacent pins.

What jumper needs to be changed before a board can change its location in a crate?
None, there is no “address” jumper. The address of a board gets specified in a software file called the “csv” file. To change the location of a board the csv file needs to be changed correspondingly, or else the softeare will not “see” the board. Remember: the MCB always needs to be in slot 1, only CBB or CAB boards can change their assigned location in a crate.

What typical software files need to exist for Monsoon to be able to run a detector?
For a detector called “myccd”, the following files should exist:

- myccd_DefaultSetup.mod
- myccd_Config.csv
- myccd_guiCategories.txt
- myccd_sequencer.ucd *(which typically results after compilation of an assembly file called myccd_sequencer.asm)*

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How is the *.ucd file generated?

The user first must create the assembly file myccd_sequencer.asm, which is basically a text file containing the desired clock “waveforms”. The *.asm file is used to derive the *.ucd file by invoking the asm4 assembler:

asm4 -d myccd_sequencer.asm myccd_sequencer.ucd

Where are voltages typically set?

In the .mod file. Example: DD_ADac, the DAC setting for the Output_Drain_A voltage could be set by the following line in the .mode file:

DD_ADac=22

Where is the range (max and min) for a voltage specified?

In the .csv file.

Where is the timing for CCD clock waveforms set?

In the .asm file (which after a compilation is available as .ucd file)

Where does one specify the (initial) voltage “rails” for the CCD clocks?

In the .mod file. Example: to set the rails for clock H1 to 8.5 V / 1.0 V the .mod file would include the following two lines:

H1HiDac=8.5
H1LowDac=1.0

Can the rail voltages be changed once the MEC has started?

Yes, by using the Attributes window.

MONSOON

What software is available to the user to run a CCD?
For systems developed in Tucson: the MONSOON Engineering Console (**MEC**).
For systems developed in La Serena: **Panview**.

How does the software (MEC or Panview) get started?
The **MEC** is started by a command such as:
mecStart myccd mypan /home/MONSOON 65
mecStart pccd ctiola /home/MONSOON 65
Panview is started by clicking an ad-hoc icon.

Can the exposure be given in milliseconds?
MEC: No, only in units of seconds. Only integer values are accepted.
Panview: Yes.

Does the basic control software allow sequences of images to be taken automatically?
MEC: No.
Panview: Yes.

In the .asm file what do the characters # and * represent?
The pound sign (#) needs to precede any variable, as mandated by the assembler.
The * indicates that a comment follows.

MONSOON

For a clock signal, how are software and actual hardware associated?
The software / hardware assignment of a clock takes place in both the .csv and the .asm files.

Example: link CCD phase H1 to CLK_OUT_00.

First attribute H1 should be assigned to CLK_OUT_00 in the .csv file. A subgroup of the columns in the .csv file might look as follows:

H1 CLK_OUT_00 0x0040000 1 0x0D000000 RDMSKWRT RDMSKWRT FLOAT UINT

Next, the corresponding lines of code in the .asm file are shown. In italic characters, are the actual .asm code lines:

***** Hardware_name CCD-signal_name***
***** CLK_OUT_00 => H1***

(Note: One or more asterisks indicate that what follows on the line is a comment).

DEF #H1 B00000000000000000000000000000001

The line above assigns the use of least significant of the 32 (hardware) clocks to H1. That is, it links hardware clock signal CLK_OUT_00 to H1, the CCD horizontal phase 1.

Hardware note: CLK_OUT_00 is actually called “C0” as it leaves the interface board via the Amp connector P2 at its pin 38 towards the CCD. Internally “C0” is derived from “CLKOUT0” (as received from the CBB by the interface board at RJ4 pin A1). And in turn “CLKOUT0” is derived on the CBB from “VCLKOUT0”. For a definition of VCLKOUT0, refer to page 8 of MNSN-EL-04-2008, the schematic for the Clock and Bias Board).

Finally, H1 can be used in a logical equation. As an example, define a logical state S_STATE1 as a function of signals RG ,the reset gate defined elsewhere, and H1 as shown in the next line:

DEF #S_STATE1 #RG OR #H1 * RG + H1

MONSOON

How does one get the ADC converter to act as if it were a 16 bit converter?
After MEC or Panview are running, in the Attributes window click on CCD_Board_Control and set DataWidth to 0x00000020. NOTE: Always press the Enter key after typing a number. To ensure that the new value has been accepted, click “Update” and verify that the correct value is displayed.

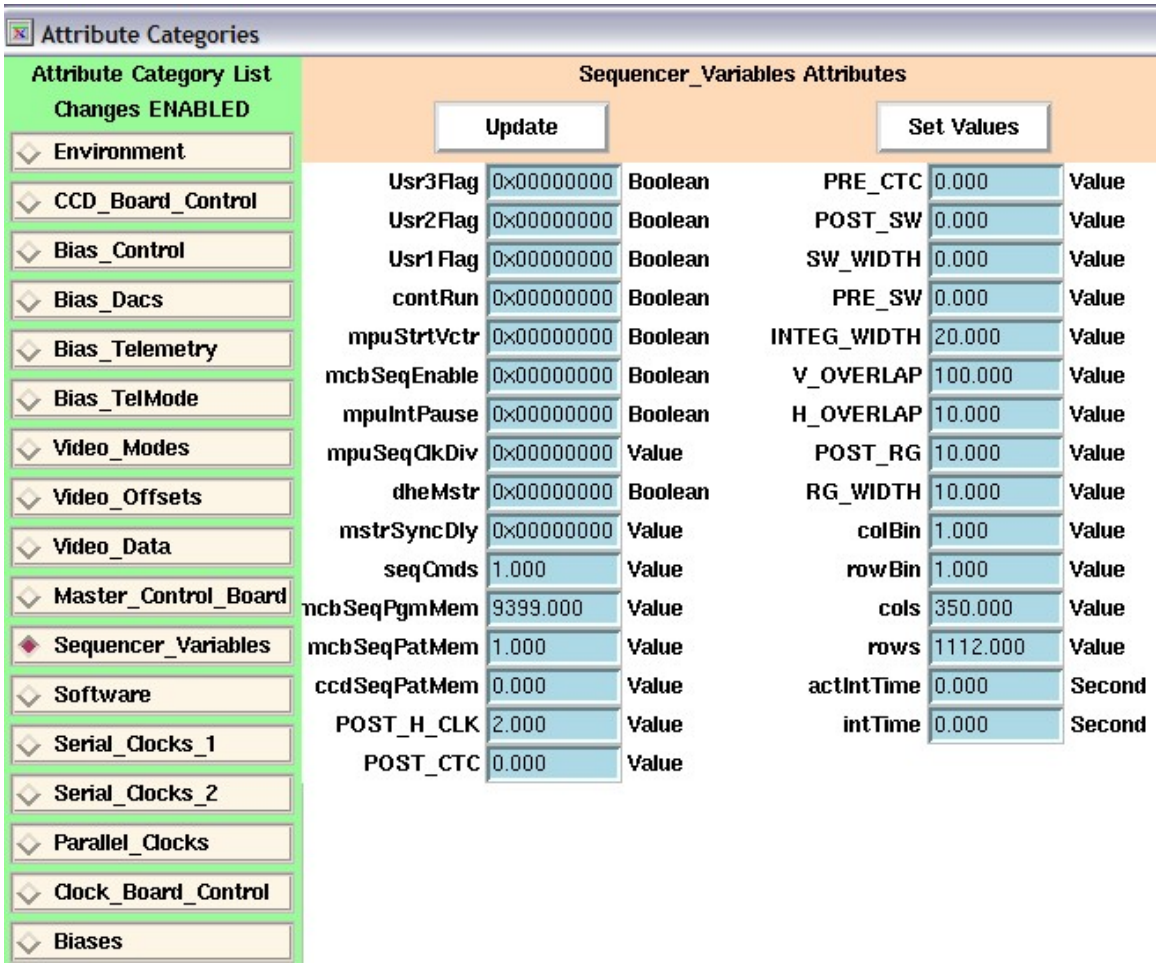
What is the typical ADC input voltage range?
For the AD7674AST converter used on the CAB, the input voltage range is set by its external reference, which is 4.7 Volts (a MAX6325 reference generates 2.5V which are buffered with a gain of 1.8879, for an output –after the OPA4277 buffer- of about 4.7 V).

How many millivolts at the CCD acquisition board input does 1 ADU correspond to?
Working backwards from the ADC:
1 LSB at the ADC input corresponds to (assume the 16 bit case) 4.7V / 65536 = 71.7 uV.
The differential driver that drives the ADC has a gain of 2 but is preceded by a resistive attenuator with a factor of 0.5, so overall this stage has a gain of 0.5 x 2 = 1.
The gain of the integrator = slope / time constant = 1000ns / 330ns = 3 approximately (here slope (or “dwell” time) is assumed to be 1 us).
The gain stage that precedes the integrator can provide gains of 1 or 2, assume the gain of 1 has been selected.
The preamp seen by the CCD output signal has a gain of 3.
So the overall gain looks like: 3 x 1 x 3 x 1 = 9, i.e. 1 LSB of the ADC corresponds to 71.7uV / 9 or about 8 uV at the input to the CAB.
For the same settings, the 18-bit case implies that 1 ADU = 2 uV at the input o the CAB.

If the CCD output sensitivity is such that 3e correspond to 8 uV, what conversion gain in e/ADU might one anticipate?

With the assumptions used before (ADC as 16 bits, 1 us slope, internal gain –preceding the integrator- of 1) 1ADU = 8 uV at the input to the CAB. But 8uV also correspond to 3e for this CCD, so the conversion gain would be expected to be about 3 e / ADU.

What does the Attribute window look like?



MONSOON: Appendix

MONSOON

MNSN-AD-01-0006_ICD_7.0_V13.1.pdf

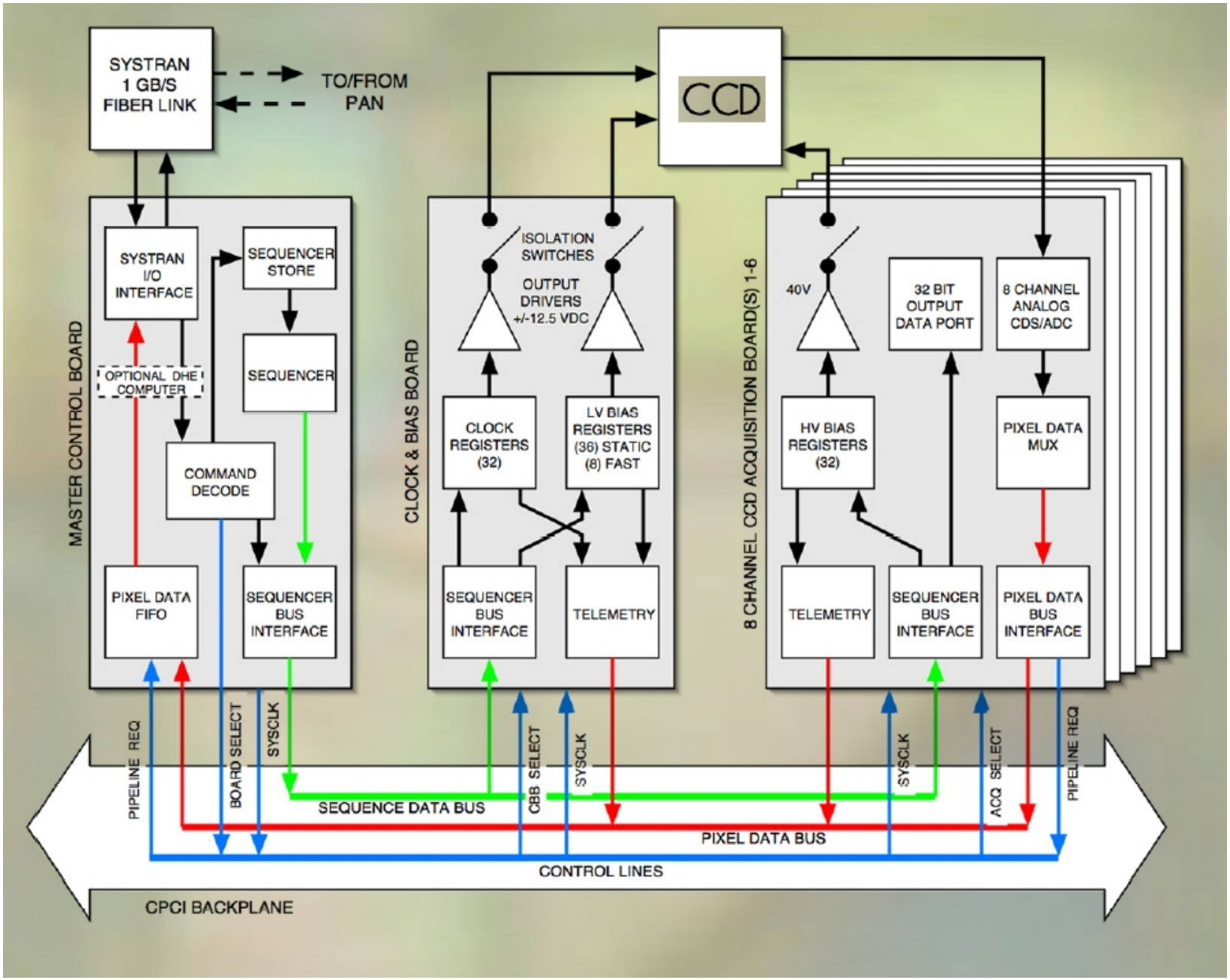
Compact PCI Backplane versus MONSOON Backplane Architectures

Only the power, ground, clock and JTAG pins have been kept as defined by the Compact PCI standard. All the other PCI signals have been reassigned. The 64-bit AD bus is reassigned as Pixel Data Bus. This bus is a generic data link from the peripheral boards to the Master Control Board. The PCI control lines have been reassigned as the Sequencer Bus. The “request” lines have been reassigned as “Serial ID”, and the “Grant” lines as “Board Select”.

MONSOON
MCB facts: 1

MCB must reside in slot 1.
PAN-DHE communication takes place via MCB.
MCB controls unidirectional Sequencer Bus on the backplane.
MCB provides a programable Sequencer.
MCB provides for clock distribution.
MCB provides for multiple-DHE synchronization.
Pixel FPGA is dedicated to data path handling.
Sequencer FPGA contains the Sequencer, decodes commands,
controls Sequencer Bus, distributes clocks.
Fiber optic bidirectional link via Systran daughter board.
Data rcvd fm PAN is always 32 bits wide.

NOAO Monsoon Block Diagram

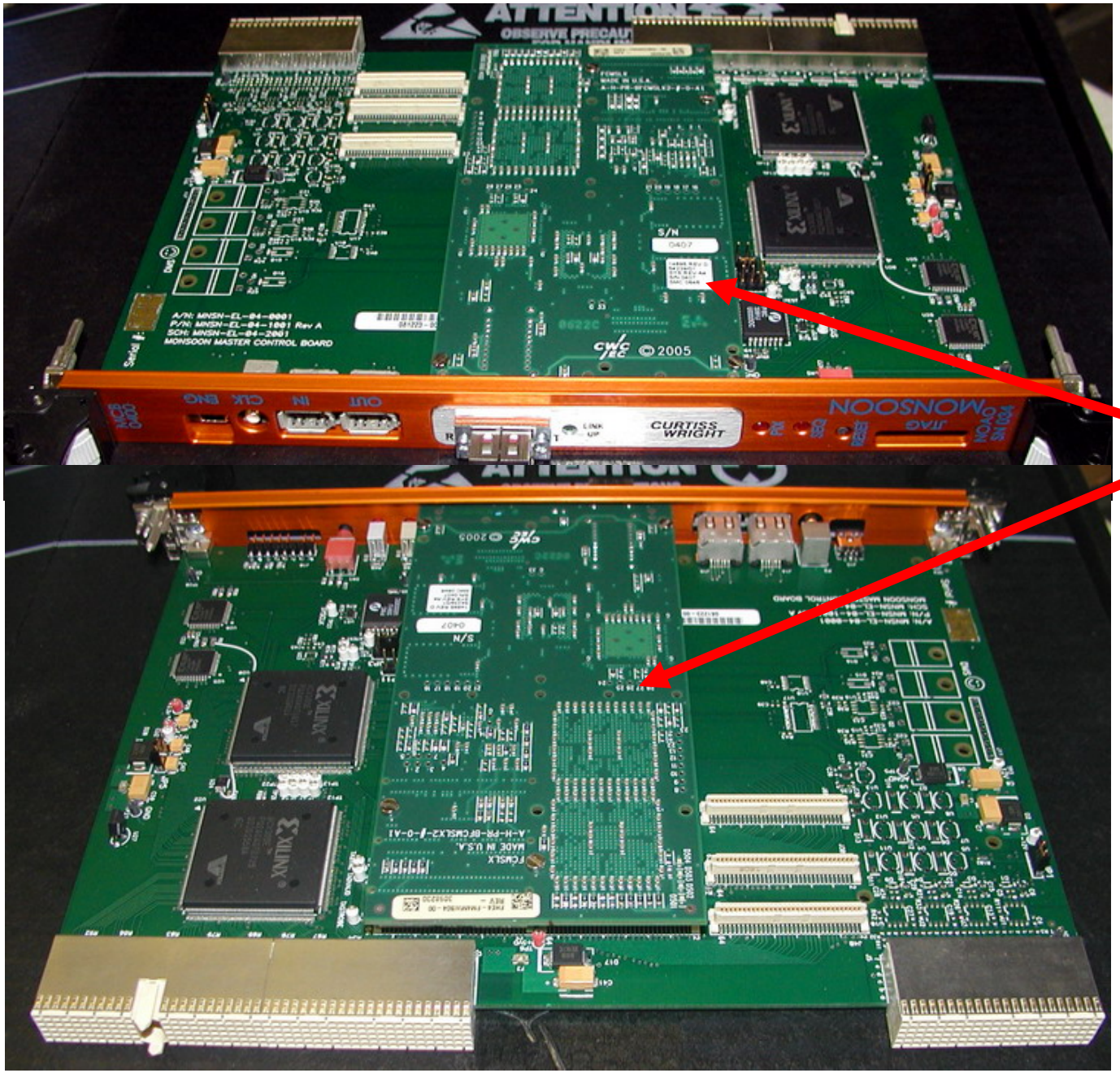


MONSOON
MCB facts: 2

Data received from PAN is always echoed back to PAN, with 2 exceptions:
- asynchronous status message always echoed after a hard boot or soft reset,
- start exposure command is not echoed.

Data to PAN: either a reply after a command or pixel data.
Messages to PAN have a synch frame appended to them.
Nominal data xfer rate is at clock rate of 40 MHz.
MCB enables/disables system clock to peripheral boards.
Write "1" to bit in "Clock Enable Register" to turn on clock source.
Sequencer bus activity is synchronous to rising edge of system clock.
Sequencer bus is unidirectional, away from MCB.
2 mode bits: reset, write32, write16, read32.
Write takes 1 clock cycle, Read takes 3 clock cycles.
Board select bits: 7. Multiple active selects are legal for write.
During a "read", pixel data bus gets latched into Pixel Bus FIFO (=128-words deep).
Pixel Data Bus is a unidirectional 48-bit bus.
Video board can burst transfer pixel data to the PAN.

MONSOON: views of MCB with daughter board

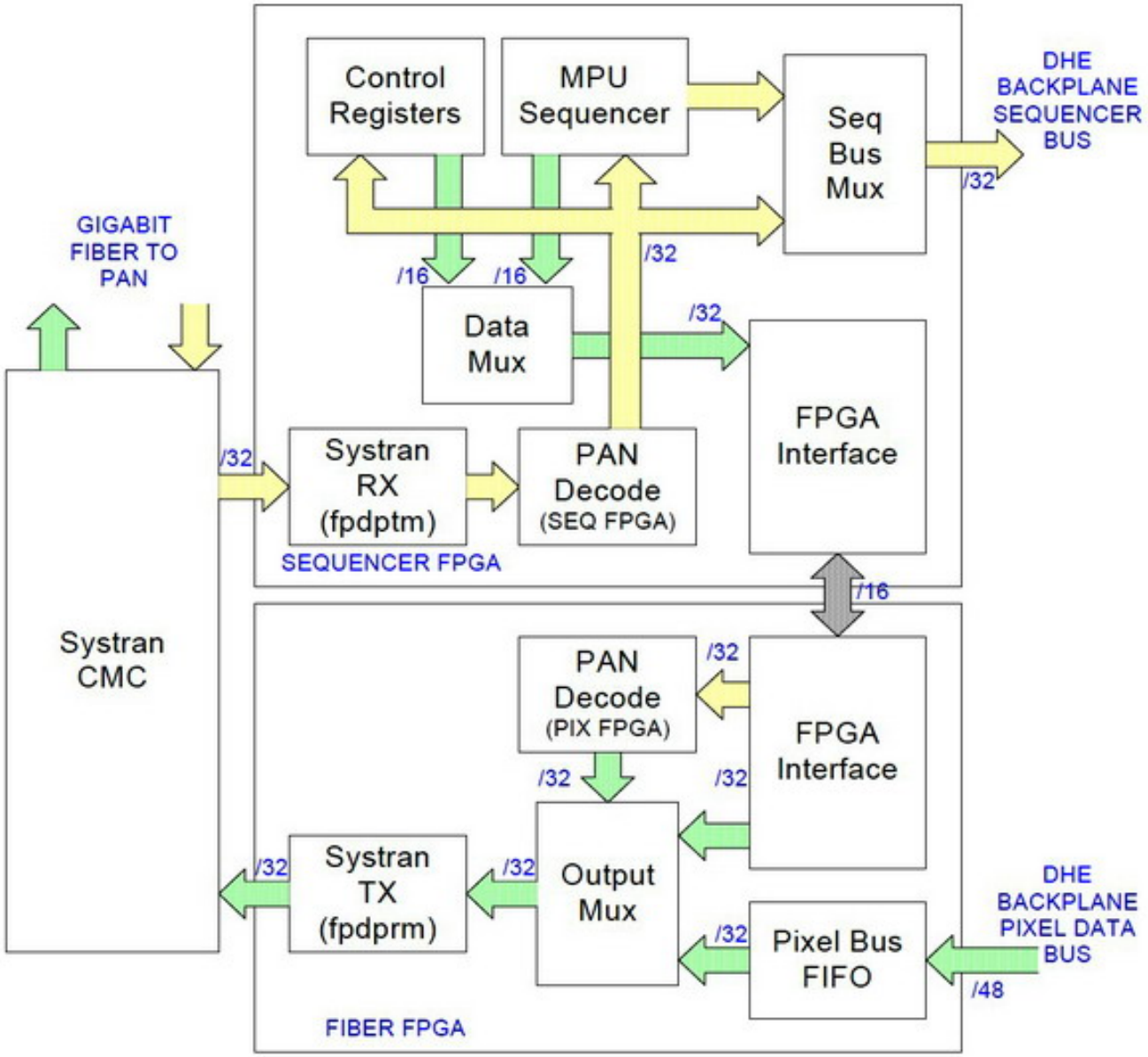


MONSOON
MCB facts: 3

2 Front Panel LEDS: one each used by Pixel and Seq. FPGAs.
Both LEDs off during power up. After booting: both LEDS on.
Asynch. command sent by PAN turns both LEDS turn off.
FP LEDs can be controlled via bits in their control registers.
Command decoding blocked until asynch. command rcvd.
Asynch. command synchronizes PAN-DHE communication.
PAN commands: asynch cmd, write, read, start exposure.

Data paths are 32 bits wide (exceptions exist).
Data received from PAN by Systran is echoed back to PAN.
But asynch status message is echoed to PAN after a Reset.
16bit data or command: PAN -> Sequencer FPGA -> Pixel FPGA.
Data for peripheral bds. are sent via backplane Sequencer Bus.
PAN operations delayed if MPU Sequencer has sequencer bus control.

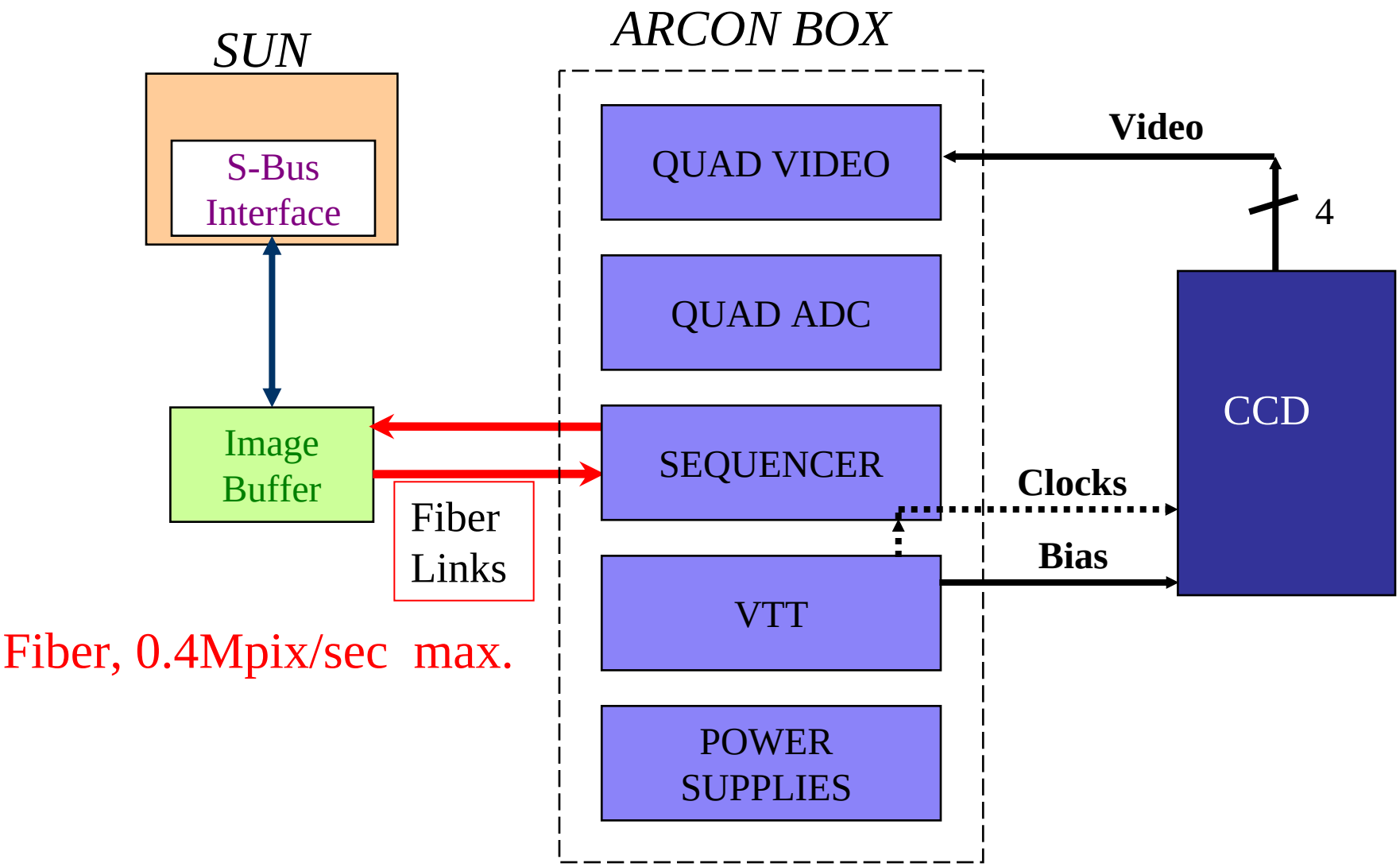
MCB data paths



MONSOON
MCB facts: 4

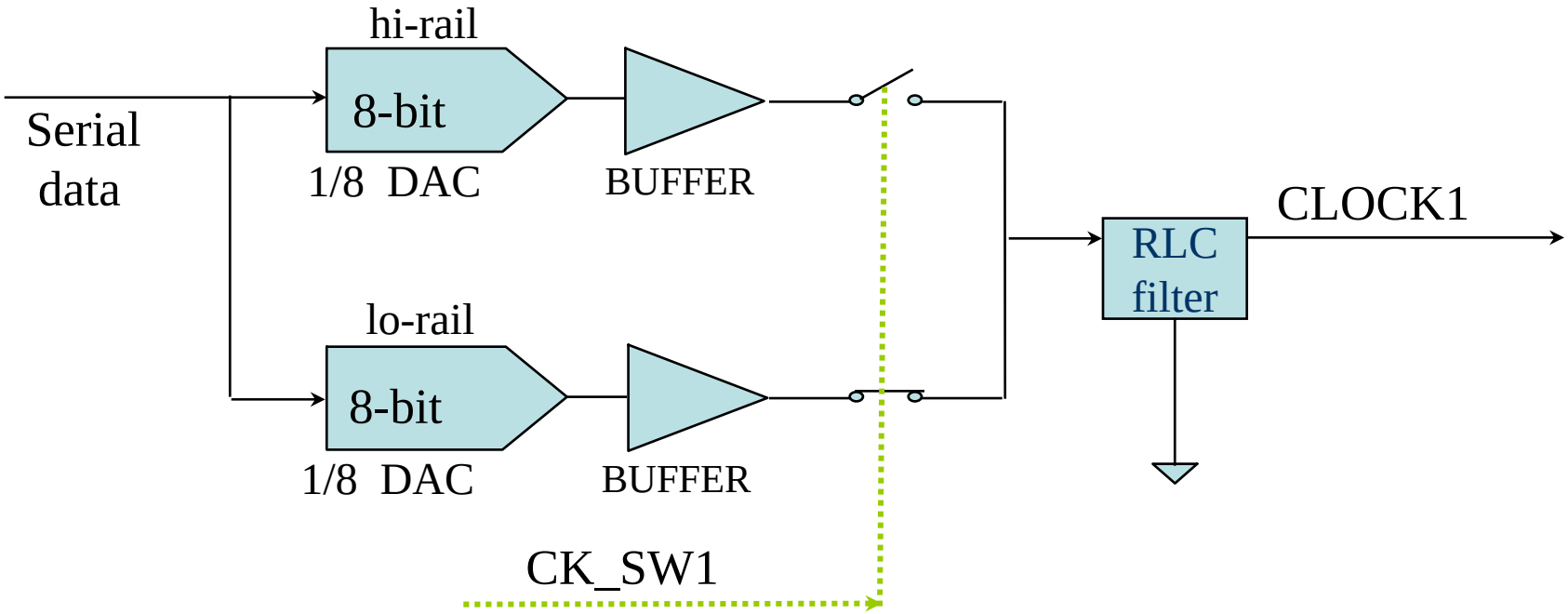
HARDWARE: Majority of logic uses 3.3 V (external or derived from 5V).
FPGA internal logic cell: requires 1.8V (derived from 3.3V).
Pixel FPGA logic: handles pixel data during detector readout.
Incoming pixel data arrive via 48-bit pixel bus.
48-bit pixel bus: allows 2 24-bit pixels or 3 16-bit pixels.
Acquisition boards can strobe data into pixel bus FIFO.
Sequencer FPGA handles control and communications.
A 32-bit FIFO is used by Sequencer to buffer 32-bit PAN data.
40 MHz master clock is used to derive individual board clocks.
MPU Sequencer:
- does not emit clock and control directly to hardware port.
- MPU Seq. -> Seq Bus Mux -> peripheral bd. control regs.
MPU Sequencer accesses addresses on Peripheral boards.
MPU Sequencer cannot access registers within MCB address space.
  Exception: the Enable Function Register (EFR).
A front panel JTAG connector provides access to EEPROMS, FPGAs.

Arcon Block Diagram

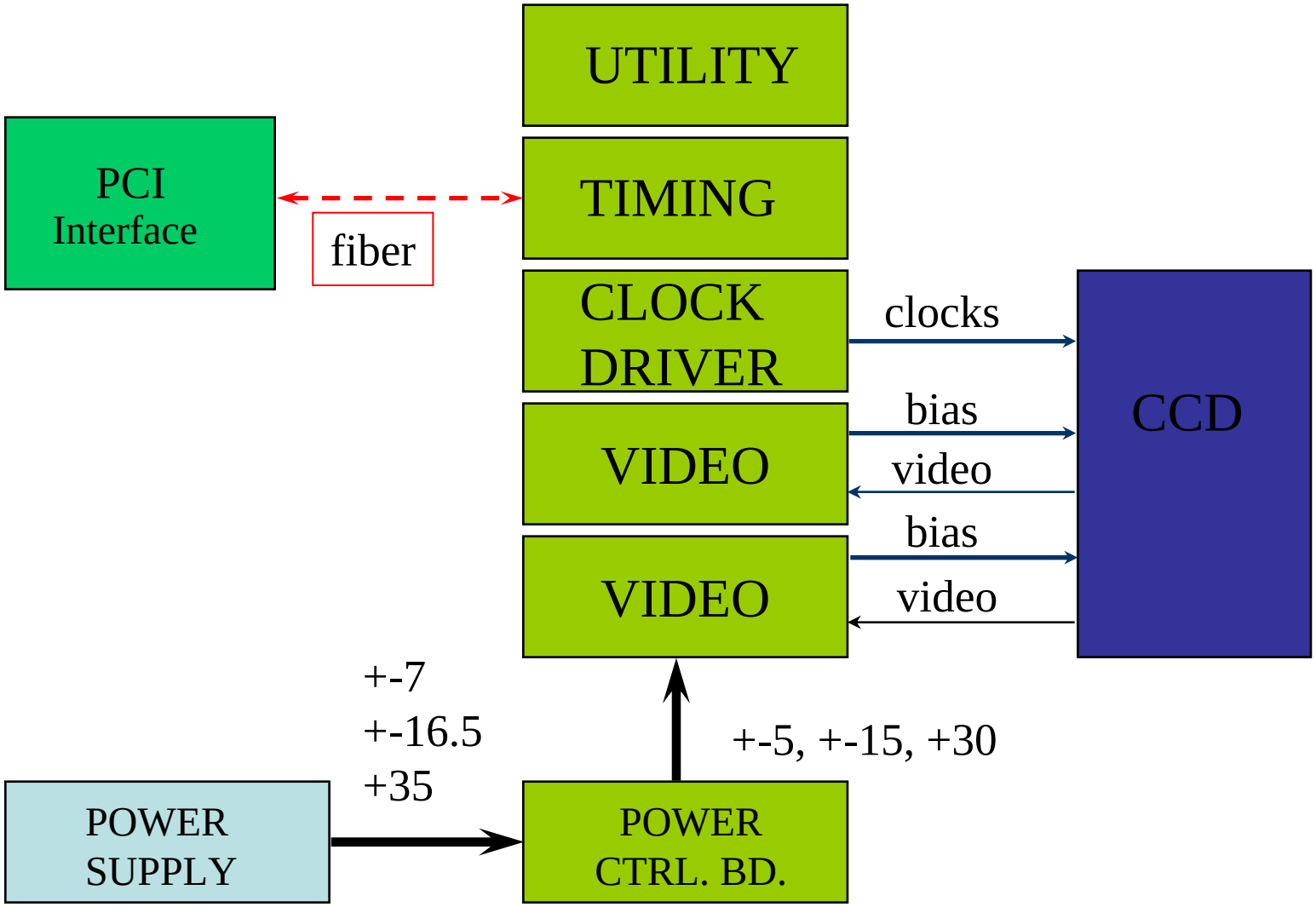


Fiber, 0.4Mpix/sec max.

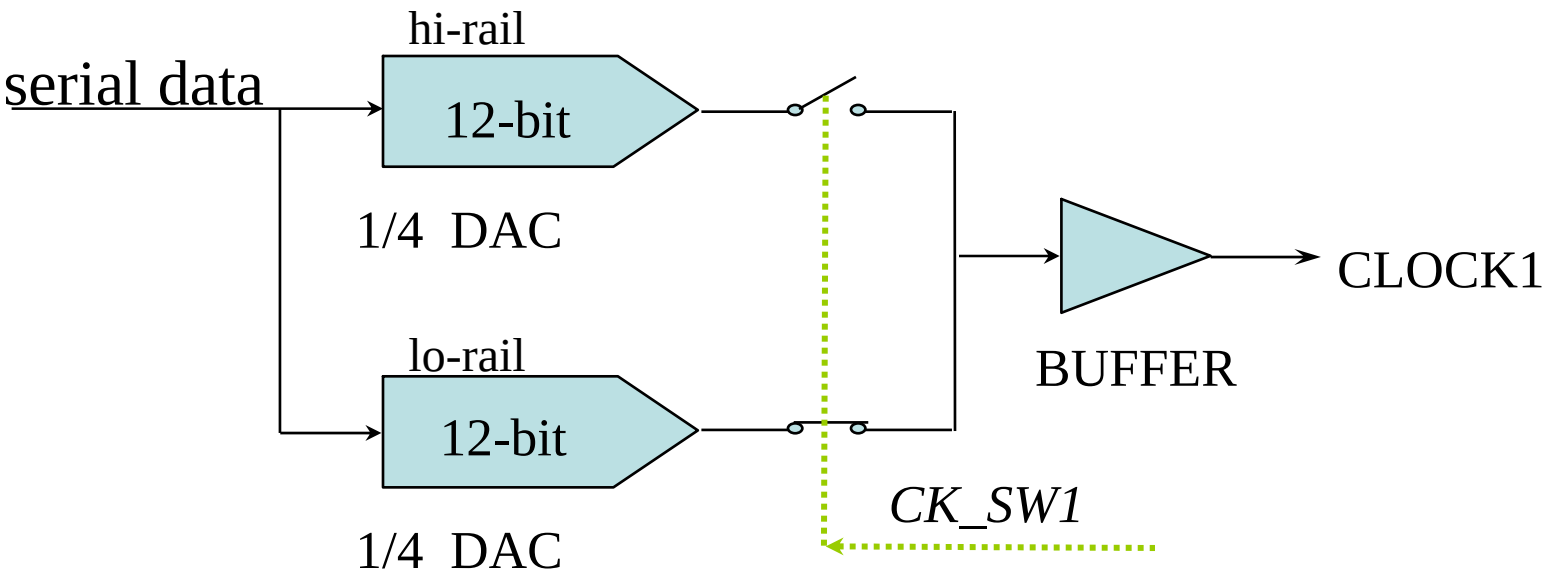
Arcon Clock Driver circuit



SDSU-2: Block diagram



SDSU-2: Clock driver circuit



- +- 10 V, 60 mA each
- 40 ns switching for 20V swing
- 2 banks x 12 clock ea., update 1 bank at a time