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TORRENT

DHE Hardware Description

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Revision History

Version	Date Approved	Sections Affected	Remarks
0	6/20/2010	All	Initial draft release - aro
1.0	7/07/2010	1,3	Added architecture, PSM Rewrite, MEZ symbol number corrections.
1.1	07/20/2012	All	Updated to reflect production hardware

Table of Contents

List of Figures

List of Tables

Preface

This document contains information relevant to the hardware implementation of the Detector Head Electronics (DHE) Hardware. Minor revisions and modifications to the capabilities and functionality of this module can be added as appendices to this document. Major modifications to the functionality of the module that would require extensive modification to this document must originate a new and separate hardware description document.

Document Scope

This document provides an overall description as well as detailed information on the hardware architecture, configuration, testing and functionality of the MONSOON Torrent DHE. It will be a valuable document to anyone who is considering, building, using, testing, maintaining or interfacing the Torrent DHE. Table 1 lists the relevant schematic drawings required to understand this document.

Table 1 - References to the Schematic Documents Referred to in This Document

Module	Designation	Section	Drawing Number	Revision
Power Supply Module	PSM	1	TRNT-EL-04-2001	-B-
Local Control Board	LCB	2	TRNT-EL-04-2002	-B-
LCB Mezzanine Board	LCB-MEZ	3	TRNT-EL-04-2003	-A4-
CCD Analog Front End	AFE	4	TRNT-EL-04-2004	-C1-
Video Flex	FLEX-VID	5	TRNT-EL-04-2005	-A-
Clock Bias Flex	FLEX-CB	6	TRNT-EL-04-2006	-A-
Transition Preamp	TSM-PRE	7	TRNT-EL-04-2007	-B-
Transition Utility	TSM-UTIL	8	TRNT-EL-04-2009	-A2-

1.0 Introduction

The Torrent DHE is divided into two main physical modules which mate via a mechanical interface that provides electrical interconnections between the two modules. There are two main modules. First, the controller module, as shown in Figure 1, contains the bulk of the electronics and performs the required functions for communications, command interpretation, and detector safety, conditioning and readout. This module is generic to the applications of Torrent within a detector type classification. There are currently two different versions of controller; one for the CCD detector class and one for the IR detector class. Each version of the controller is common for all detector types within that class. Second, the transition module, as depicted in Figure 2, provides the mechanical and electrical interface to the controller module and detector. This module houses the low noise preamplifiers, clock and bias signal conditioning, detector safety features and temperature sensing circuitry to interface to the generic controller modules. The transition module is designed to be physically and permanently mounted to the detector Dewar.

Figure 1 - Torrent Controller Module

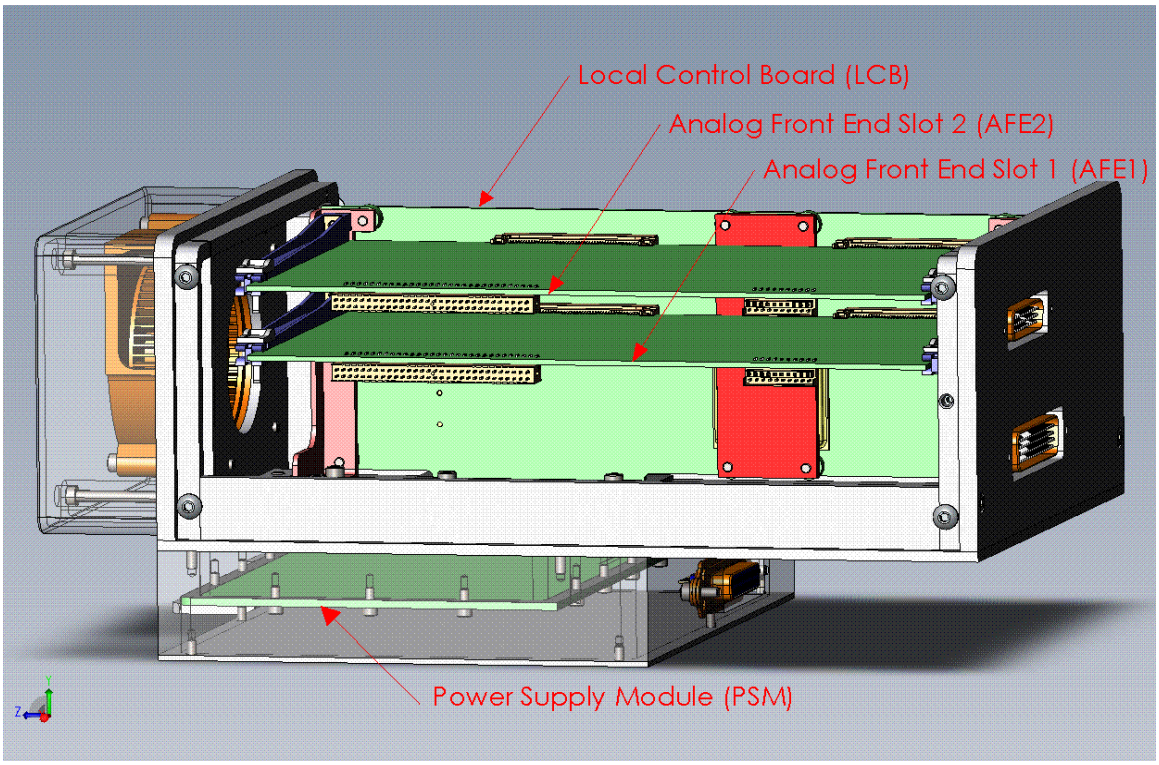
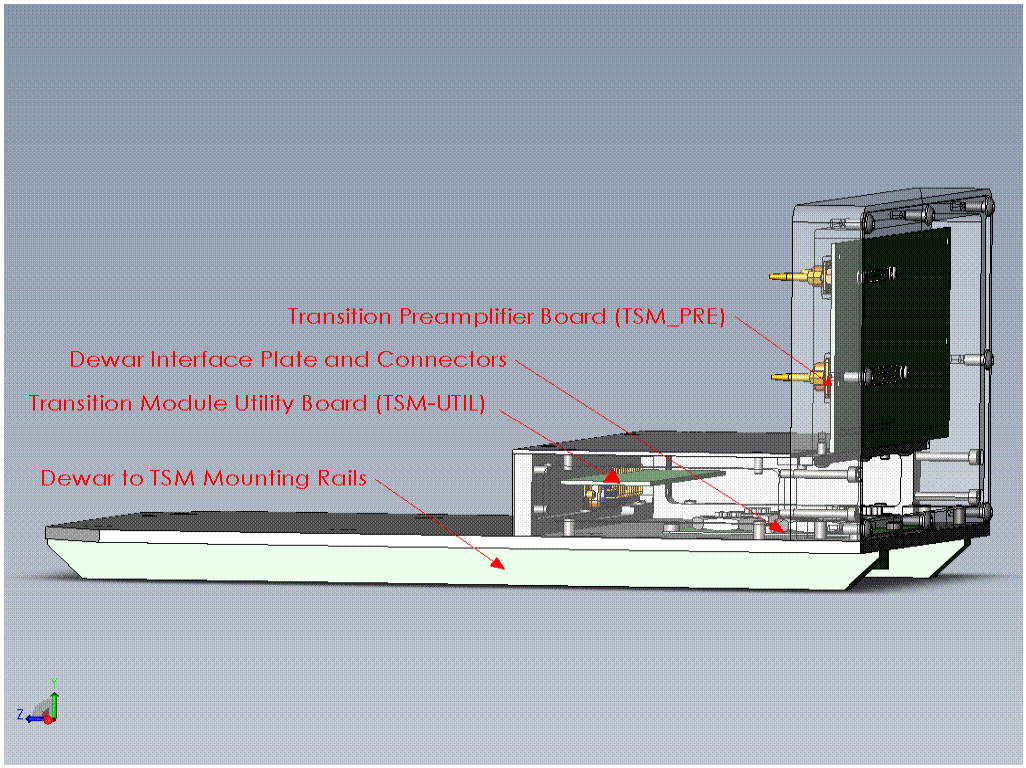


Figure 2 - Torrent Transition Module



1.1 Variants of the DHE

Two variants of the DHE can be built; one for CCD detector technology and one for IR detector technology. At present only the CCD variant is in production. The two variants differ in their use of specifically designed AFE, Flex and Preamplifier boards. The PSM, LCB and TSM_UTIL components are common to all variants.

The CCD variant of the Torrent DHE is equiped with capabilities to support a single CCD detector or a small array of CCD detectors with up to a total of eight video signals. Each controller module is equipped with two AFE boards that can be independently powered on or off. Each AFE is designed to support P-Channel or N-Channel detector devices. The power supply has provision to generate back side bias potentials for deep depletion mode detectors (Vbb).

The variant type is detected during the power-on sequencing by a strapping difference on the AFE board **AFE_SCL_SRC** signal. This detection allows one of two possible versions of firmware to be loaded during power on sequencing to facilitate AFE control. The variant selection is described in Table 2.

Table 2 - DHE Variant Selection

Variant	AFE Signal AFE_SCL_SRC Impedance to Ground.	LCB Eeprom Revision
IR	10.0K	0
CCD	Open	1

1.2 Firmware Component

Much of the DHE hardware and functionality is controlled by firmware that is loaded into a single Xilinx Virtex 5 FPGA during the power on sequencing. The description of the firmware can be found in the Firmware Users Guide - document number TRNT-EL-08-0010.

1.3 Hardware Architecture Description

The complete DHE is built from eight printed circuit board assemblies. These assemblies are connected together in a heirarchy by physically mated connectors that dramatically reduce point to point wiring. The printed circuit board assemblies that make a complete DHE are:

Power Supply Module (PSM) –generates the majority of the power supply potentials required by the system and is described in Section 2.

Local Control Board (LCB) –contains all the required logic to perform PAN communications, power supply control, detector clock and video processor sequencing, telemetry, and video and configuration memory management. This module plugs into the PSM and is described in Section 3.

Local Control Board Mezzanine (LCB-MEZ) –controls the enabling and protection of the power supplies used by the Analog Front End boards. This board also contains supply current measurement telemetry for each AFE. It is described in Section 4.

Analog Front End Board (AFE) – up to two examples of this board plug directly into the LCB and provide the generation of bias and clock voltages, telemetry and video processing functions. This board is described in Section 5.

Video Flex Circuit (FLEX-VID) - another passive and flexible printed circuit used to connect the AFE board(s) to the transition module. This circuit carries the video signal after preamplification in the transition module and is described in Section 6.

Clock and Bias Flex Circuit (FLEX-CB) – this passive and flexible printed circuit connects the AFE board(s) to the controller module connecters that mate with the transition module connectors. This circuit carries the clock and bias signals and is described in Section 7.

Transition Module Preamplifier board (TSM-PRE) – this circuit is mounted in the transition module and provides the video signal preamplification, breaks out the clock and bias signals to allow wiring to the Dewar connector panel, and provides a site for hardware detector safety component mounting. It physically carries the connectors that mates to the clock and bias and video flex circuits. The TSM-PRE is described in Section 8.

Transition Module Utility Board (TSM-UTIL) – a small circuit board that carries the conditioning circuitry for measurement of diode or PT100 temperature sensor devices mounted close to the detector in the Dewar. It also routes the detector heater connection and shutter and preflash control signals available for point to point wiring to the Dewar connector panel. The TSM-UTIL mates directly to the PSM via a bulkhead connector. It is described in Section 9.

Dewar Connector Panel (DCP) – a galvanically isolated plate made from FR11 material and used to mount the connectors to provide the Dewar electrical feedthrough to the detector. It is generally built on an individual basis to match the physical spacing and type of connectors mounted to the Dewar that is used for any particular instrument. It is described in Section 10.

2.0 Power Supply Module (PSM)

Refer to schematic TRNT-EL-04-2001, page 2.

This description corresponds to the Revision –B– power supply hardware.

The PSM module supplies the primary voltage potentials with sufficient current to allow the DHE logic and analog circuitry to function as designed. The power input and output specifications for the PSM are listed in Table 3.

Table 3 - PSM Power Input/Output Specification

Designation	In/Out	Voltage Range (V)	I Nom (ma)	I Max (ma)	Description
INPWR_VRAW_P	INPUT	22 to 26	1000	2500	Power input
VCC	OUTPUT	+3.3	1130	3000	Logic supplies only
VFAN	OUTPUT	+7 to +14	300	400	DHE cooling fan, variable flow
VANA+	OUTPUT	+5 to +11.5	400	720	Video processing circuits +ve rail
VANA-	OUTPUT	-11.5 to -5	250	720	Video processing circuits -ve rail
VCB+	OUTPUT	+9 to +18	350	650	Clock and low voltage bias +ve rail
VCB-	OUTPUT	-18 to -9	350	650	Clock and low voltage bias -ve rail
VHV+	OUTPUT	+30 / +5	120	200	High voltage Bias +ve rail
VHV-	OUTPUT	-5/ -30	120	200	High voltage Bias -ve rail
VBB	OUTPUT	+/-8 to 75v	2	10	Back side bias supply
VHTR	OUTPUT	+22	275	500	Cryostat heater current regulator supply into 40 Ohms nominal.

With the exception of the **VCC** supply, the separate power supply output voltages are adjustable by the user to allow power (heat) dissipation to be reduced at the cryostat site. The supplies are set to a voltage to provide just enough head room for the required dynamic range of the control circuit for a particular detector application. All supplies have telemetry capabilities to monitor voltage and current, except the **VBB** supply where no current telemetry is available.

The **+/- VANA** and +/- **VCB** power supplies are provided with servos that use the supply telemetry to correct for low frequency drift due to temperature and aging effects.

The **VFAN** and **VHTR** power supplies are provided with servos using relevent temperature sensors to stabilize the DHE and detector temperatures respectively.

2.1 Implementation of the PSM

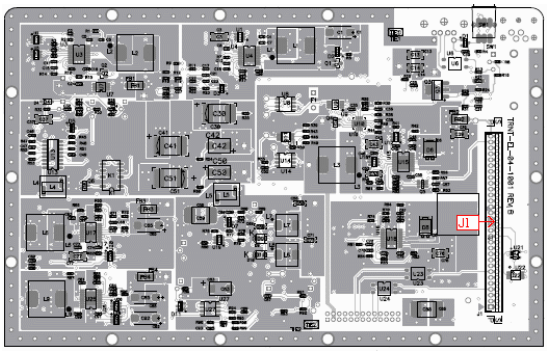
Refer to schematic TRNT-EL-04-2001 page 2.

The PSM is housed in a separate enclosure that attaches to the bottom of the controller module housing. Access is by way of a cover plate on the bottom of the Controller Module when the controller and transition modules have been seperated. Figure 1 shows the relative placement of the PSM within the Torrent controller module. The power supply can be seen mounted in the lower part of the enclosure.

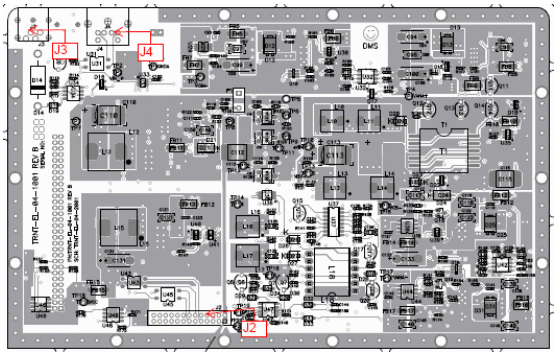
Having the power supply in a separate compartment helps attenuate any EMI interference produced by the switch mode power regulators in the PSM from influencing the low noise circuitry of the controller. This arrangement also provides for a conduction cooling path for the PSM to dissipate heat to the controller chassis through the printed circuit board. This circuit board has a layer dedicated to thermal conduction of heat away from the components to the edges of the board.

The PSM consists of one printed circuit board assembly with four connectors. Table 4 shows a plan view of the top and bottom of the PSM PCB. The four connectors provide for the PSM to connect to the primary power source (J3), the Local Control Board (J1), an optional power control and ground routing connector (J4) and the to the Transition Module (J2).

Figure 3 - Supply Connectors



PSM Top view



PSM Bottom view

The DHE power supplies are generated using three basic types of regulator topology: (1) Positive Buck regulation for positive voltages below the primary voltage supply magnitude, (2) Inverting Buck regulation for negative supplies below the primary voltage magnitude, (3) Isolated push pull transformer coupled design when the required output voltage is above the magnitude of the primary supply, and (4) the detector heater supply which is a current regulator driving a resistive load used to heat the detector and maintain detector temperature control.

All of the power supplies are designed to run in continous mode and to be synchronous to each other and slaved to the pixel conversion frequency. This is designed to minimize the inductor current slew rates and channel the power of the switching transients and ripple currents into the fundamental or a harmonic of the pixel conversion rate of the DHE. When this is achieved, any conducted EMI from the power supply or supply voltage ripple will appear on the output of the video processor as a simple dc offset that is common to all pixels and therefore not seen as a pixel value variation i.e. noise.

2.2 DHE Power and Ground Distribution Scheme

Refer to schematic TRNT-EL-04-2001, page 2.

This page shows the general connection scheme for the power supply and ground network. Primary (24v) power is supplied to the regulators to develop the individual potentials required by the design.

The PSM has a single massive ground plane that is used to tie the return current paths from the regulators to the primary power negative return path. This point, which is the primary power negative rail where it enters the PSM, is considered the electrical reference point of the DHE and is called generically the ‘power ground’ **(PWR_GND)**. The DHE chassis ground **(CHASSIS_GND)** is isolated

internally from the **PWR_GND** and is fed through and bonded to the transition module. All panels and parts of the DHE chassis are electrically connected to provide shielding and protection to the detector.

NOTE: The power ground and DHE chassis ground must both be bonded to the telescope and electrical supply 'safety' ground at some point.

The usual practice is to find a known 'quiet' place on the instrument or telescope structure to make this connection. There are pins available in the PSM remote power control connector (J4) to facilitate taking these ground points out of the DHE for this purpose.

In addition to the **CHASSIS_GND** and **PWR_GND,** there are three conductor paths that are designed as shield sink connections. These three conductors are bonded to the **CHASSIS_GND** point at the remote power control connector and are available as three separate shield points for cables and/or Dewar grounding points in the transition module.

The primary power is conditioned by a circuit that protects the DHE from under voltage and over current conditions. When this circuit is active it switches off the primary power to all regulators and illuminates a yellow indicator in the power switch.

When the DHE power switch is activated, the power supply produces only the VCC logic supply to the LCB via J1. The LCB has local regulators on board to produce the logic supplies required by the LCB. All other power supplies are held disabled until the primary power on sequence has completed. This sequence includes the successful loading of the Virtex FPGA from its eeprom code store. At this point the power supply is capable of being controlled by the LCB.

The analog power supply group consists of the regulators **VANA+, VANA-, VCB+, VCB-, VHV+, VHV-**, and **VBB**. With the exception of the **VBB** supply, the analog supply group is routed through the LCB power connector (J1) and directly to the LCB-MEZ via isolated traces on the LCB. The power ground is split on the LCB at the PSM / LCB power connector to provide a separate return path between the LCB logic power return and the analog power return. The LCB-MEZ further splits the analog ground path into two separate paths, one for each AFE position. This concentrates the return currents from the AFE, TSM-PRE and detector at the LCB power connector and minimizes the risk of ground loops by providing the lower impedance return path back through the board hardware that supplied it.

There are three power supply enable signals developed by the LCB that control the analog power group. These signals (**VANA_ENBL, VCB_ENBL**, and **VBB_ENBL**) are used to selectively power on the regulators depending on the requirements of the detector. The **VHV** regulator is enabled by the **VCB_ENBL** signal. This allows savings in power dissipation and prevents a regulator from running in non-continous mode when unloaded.

The **VHV** and **VBB** regulators are designed to support both P-Channel and N-Channel CCD detectors. To allow this there is a relationship of the polarity between them. When P-Channel mode is selected (VHV_POL_SLCT = low) the **VHV** regulator develops a negative high voltage drain bias supply of –30v and an amplifier low end biasing voltage of +5v. In this mode the **VBB** supply generates a high voltage potential between +10v and +75v. In N-Channel mode (VHV_POL_SLCT = high) the **VHV** regulator generates a positive high voltage supply for drain bias supplies of +30v and a –5v amplifier potential with the **VBB** supply generating a negative high voltage between –10v and –75v. The **VBB** supply is fed through to the transition module utility board (**TSM-UTIL**) directly from the PSM via J2 and has a separate return path to reduce ground noise on this supply.

The VFAN supply is used to control the rotation speed of a DC blower to control the internal temperature of the electronics. The blower is installed in the controller module enclosure and uses circulated air to carry generated heat away from the circuit boards using convection. The chassis skin is used to carry this heat away from the DHE by convection and/or conduction paths.

The VHTR supply is used to control the current fed to a resistor (nominally 35 Ohms) that is mounted in close proximity to the detector in the cryostat. This supply is fed directly to the transition module via J2 to reduce the number of connectors that it has to pass through. This supply has a maximum capacity of 10 Watts at about a 22v potential. The maximum power can be limited by selecting an appropriate strap option on the TSM-UTIL board.

2.3 DHE Power Connector

Refer to schematic TRNT-EL-04-2001, page 3.

The DHE requires an external 60 Watt, 24 Volt DC primary power source. This is usually a commercially available switch mode power block, such as Astrodyne part **SPU60-108,** with a modified connector . The external power supply connects to the DHE via a **RP34-8SP-4S** female connector available from Hirose, which is a straight plug. A right-angle power cable plug is available as part number **RP34-8P-4S**. The matching male connector (J3) mounted on the power supply module is part number **RP34-8R-4PDL** from Hirose.

Two connector pins are used for each conductor of the power supply cable. Odd number pins are positive, even numbered pins are negative polarity. The nominal operational voltage range for the power supply is between 22v and 26v. Reverse polarity and over voltage protection (at 32v) is provided by the power supply. Input voltages under 22v will shut down the power supply and continously illuminate the power-on pushbutton with a yellow LED.

2.4 Power Protection Circuit

U34 is employed to monitor the primary power voltage and current. Input power reversal protection is provided by D19 that will not allow the series pass MOSFET Q3 to turn on if the input potential is reversed.

The resistive divider formed from R114/R115 is used to detect input voltages below 22v and inhibits the turn-on of the series pass MOSFET Q3. This occurs when the voltage of U34 pin 1 is below 3.6v. Once a voltage of greater than 22v is sensed, U34 ramps up the potential of the gate of the MOSFET to approx 10v above the primary supply voltage to turn on Q3. At this point the switch controller U33 is enabled and the VCC regulator comes up to standby state. The current consumed by the DHE is monitored by R21. If the potential across this resistor is above 50mv for more than 4ms then U34 will shut down the drive to the gate of Q3. This forcefully switches off the complete DHE. Under this condition the push button switch is illuminated with a yellow LED and the power must be unplugged to reset the circuit.

C13 and C14 provide bulk capacitance and isolate the PSM from any inductance of the primary power source caused by cable inductance.

2.5 Grounding and Remote Power Control Connector

Refer to schematic TRNT-EL-04-2001, page 3.

Each application of Torrent to a particular detector and instrument may require a unique local grounding scheme for the DHE chassis, shield and power grounds. Connector J4 is provided to bring out the chassis and power ground connections of the DHE. The power and chassis grounds are only connected together in the DHE when the controller part of the DHE is removed for maintainence and other actions. This connection is provided for by a small switch mounted on the transition module (TSM) to provide protection to the detector when the controller is disconnected. **The power ground for the DHE must be connected to the chassis and telescope or instrument ground at some point**. If it is left floating there will be no control over the potential difference between the chassis (safety) and power grounds. J4 provides a means to connect these grounds together either at a remote point such as a quiet ground point on the instrument or a simple jumper within the connector mated to J4 when the chassis ground connection is made mechanically.

J4 also provides the means to remotely control the power to the DHE and to monitior the power status. Each of these power control and status signals is isolated from the DHE ground via an optoisolator to preserve the DHE grounding integrity. Table 4 shows the power control signals.

Table 4 - Grounding and Remote Power Control Signals

Pin	Signal	Description
1	**REMOTE_PWR+**	Remote power control +ve
2	**REMOTE_PWR-**	Remote power control -ve
3	**PWR_STATUS+**	Power status +ve
4	**PWR_STATUS-**	Power status -ve
5	**INPWR_VRAW_N**	Power ground
6	**GNDE**	Chassis and shield ground
Shld	**GNDE**	Chassis and shield ground

J4 interfaces to a standard 6-pin MiniDin male plug such as CUI Inc. **MD-60**. The remote power control signals use the same switch controller as the DHE power switch and function in the same way.

To power on the DHE remotely, apply approximately 5ma of current (vf approx. 1.2v) for more than one second through the **REMOTE_PWR** connections to energize the optoisolator (U6) and start the power-on sequence of the DHE. This occurs approximately one second after the optoisolator is energized. Once the DHE power up sequence is complete, the open collector pair of the **PWR_STATUS** signals generated by U31 will become low impedance to indicate that the DHE is powered on. Once power-on status is detected the current through the REMOTE_PWR connections can be removed.

To remotely power down the DHE, energize the U6 optoisolator again by applying a forward current to the **REMOTE_PWR** signals for greater than three seconds. Monitor the **PWR_STATUS** signals until the open collector pair goes high impedance signalling that the DHE power off sequence has been completed. This occurs approximately three seconds after the optoisolator is energized. Once the powered down status is received, remove the energizing current from the **REMOTE_PWR** connections.

2.6 DHE Power Switch and Power Status Indication

Refer to schematic TRNT-EL-04-2001, page 3.

DHE Power is controlled by a small push button switch (**SW1**) mounted on the power supply. The switch acts as a power-on button when the DHE power is off and a power-off button when the DHE is powered on.

When the DHE is powered down, pressing the switch and holding it pressed for approximately one second will initiate a power-up sequence of the DHE. When the sequence is initiated the VCC power supply is switched on and the green indicator light (mounted inside the switch body) will illuminate. Releasing the switch will extinguish the indicator and maintain the DHE power in the **on** state.

While the DHE is powered up, pressing the switch again will illuminate the green indicator light immediately. Holding the switch depressed for approximately three seconds will initiate a DHE power-down sequence and the indicator will extinguish while the switch is still depressed. Release the button at this point to maintain the DHE in a powered down state.

DHE power status can be monitored by momentarily depressing the switch and observing the green indicator. If power is on then the green indicator will illuminate while the switch is pressed for this short period, which would be less than the power-down delay time.

The switch also has a yellow indicator that illuminates if either the 24 Volt DC primary power source is faulty, that is, supplying less than 22 Volts, or if an overcurrent event activates the protection circuitry.

U33 provides a debounce and delay circuit for the push button switch. When the primary power is present and the DHE is powered off U33 pin 6 is clamped to ground which holds the VCC regulator in standby mode. When the push button switch is activated for a period of time set by C1 (approx. 1 second) U33 will release pin 6 and enable the VCC regulator to go to active mode. When the pushbutton switch is activated while the DHE is powered up, U33 pin 5 is pulled low. This signal is used to advise the Virtex FPGA on the LCB that a power down has been requested. The FPGA then has enough time to complete an orderly shutdown before the VCC regulator is put back to standby mode by pin 5 being pulled low. The FPGA can request a shutdown at any time by setting U33 pin 8 low. C2 controls the time that the pushbutton must be held on during a power-down event before the INT signal is sent to the FPGA. It is set to nominally three seconds.

2.7 VCC Positive Buck Regulator

Refer to schematic TRNT-EL-04-2001, page 4.

All positive supply voltages that are below the primary potential of 22v are generated using a common Buck regulator design. This explanation will use the VCC regulator as an example of the generic qualities of the design.

The National Semiconductor LM25576 controller (U18) with internal switching MOSFET and external diode is used as the basis for the buck control. This device accepts up to 42v maximum input voltage on the VIN pins (3 and 4), which is required for the inverted regulator circuits since the sum of the input and output voltages appear across the switch in this configuration. This device also allows a wide range of switching frequencies and has a relatively easy-to-use feedback loop compensation scheme.

There are other versions of the same buck controller architecture (LM25574, LM25575) that have a smaller package and lower output power capacity (but still suitable for some supplies). However, the design uses the LM25576 controller part for all supplies to reduce the number of component types and to take advantage of the extra efficiency, due to lower switch Ron, which this part offers.

U18 develops and internal bias voltage that appears on VCC pin 1. This voltage (approx. 7v) is available when the shutdown pin 2 is above 0.7v. The shutdown pin has a 5µA pull-up current source that sets this pin's potential at approximately 1v using R70 when the regulator is disabled. Under these conditions the analog switches U40 and U41 are powered from internal bias voltage on U18 pin 1 and the U18 is in standby mode.

When the enable signal (U40:6) is set above the switching threshold of U40 (2.4v), the regulator internal bias voltage potential is fed to the voltage divider formed by R74/R70 and half of this potential is seen at the shutdown pin thus turning on the regulator. When the enable signal is set low, U1 opens and the regulator goes back into standby mode using the regulator shutdown pin current to set the voltage at 0.82 volts.

When enabled, U18 develops a pulse width modulated waveform (PWM) at the SW pins (17 and 18) that periodically injects a charge into the inductor L15. This charge is mainly delivered from the input capacitor C121 and the from the primary power supply. The inductor stores this charge and begins to transfer the energy to the output filter capacitors C76 and C131 and to the load. During the off period of the switching waveform, the regulator side of the inductor is now coupled to ground via diode D8, and through an internal current sensing resistor between the IS pins (15,16) and the PGND pins of the regulator (13,14). This allows the regulator to monitor the change in current flowing from the inductor into the capacitors and into the supply load. This measurement is then used in combination with the voltage feedback sense pin (7) to modulate the pulse width to maintain a constant output voltage. The feedback voltage is developed from the voltage divider R11/R12 to present a voltage of 1.225v on the feedback pin (7) when the ouput voltage is at the required value. Components R81/C72 and C75 are used in the feedback loop of the internal error amplifier and form a simple integrator to regulate the pulse width of the switching waveform. The value of the compensation pin (6) should track the value of the feedback pin (7) during normal operation when this value is between 0.7v and 2.1v.

NOTE: A more detailed account of buck regulators can be found here and of the LM25576 device here.

The frequency of this periodic signal is determined either by the timing component of the regulator (R85) or by the application of a negative pulse to the synchronization pin (5). This synchronization pulse is generated, when enabled to do so, by the Virtex FPGA on the LCB. It is a square wave with a frequency greater than the free running regulator frequency and at a frequency that is synchronous to the pixel acquisition rate. This is important to enable the removal of the regulator switching noise and ripple from the detector video signal. U41 is provided to buffer and normalize the synchronization clock so that it may be applied to the positive and negative regulators with a minimum difference in propgation delay.

The inductor size (L15) for all regulators is a major factor in the determination of the output ripple, the efficiency and the switching frequency. The choice of inductors for each regulator was made to best fit to the minimum input / output differential at the lowest PWM switching frequency while minimizing the DC losses and size of the inductor.

The input capacitor type and size (C121, C123) for the regulators is based on the available high value / high voltage capacitors to handle the local ripple current with low ESR to reduce reflected switching artifacts from reaching the other supply regulators.

High Ohm ferrite beads are used on the input (FB13) and output (FB15) of each regulator to supress any spurious high frequency switching artifacts caused by board layout and device parasitics.

Components C61/R64 are used to snub the parasitic voltage spike that occurs between the time that the regulator switches off the drive to the inductor on pins 17 and 18 and the time when the diode D8 begins to conduct.

During operation the LM25576 regulator will be dissipating approximately 70mw develop the regulator internal supply on pin 1. Alone this would not account for much however there are six such regulators used in the PSM, which equates to a total of approx 0.42 Watts. In the design, transistor Q10 allows the regulator to use the VREG supply generated by the VANA+ regulator when it is enabled and set to 8v or above. This allows a reduction in the power dissipation of each regulator to approximately 12mw with a system saving of approx. 0.35 Watts.

2.8 VFAN Positive Buck Regulator

Refer to schematic TRNT-EL-04-2001, page 5.

This regulator is based on the basic VCC regulator design described in the previous paragraph with provision for adjustment of the output voltage. The output voltage of the regulator is set by resistive divider R56/R61 to be 14v. The adjustment is provided by the potential seen on U15 pin 11, the soft start pin. During normal operation this pin supplies a current to the attached capacitor when the regulator is enabled to provide a slow ramp of the output voltage. Once the startup is complete this pin normally has a potential of 1.225v, which is the potential used as the reference for the internal error amplifier. Q5A provides a current path that is nominally 0.6v above the potential on C55. This is used to modulate the error amplifier reference by using a 3.3v pulse width modulated signal from the Virtex FPGA. This signal is scaled by resistors R57/R63 and integrated on capacitor C57 so the output of the regulator tracks the potential on U15 pin 11 which is modulated by the PWM control signal.

2.9 VANA+ Positive Buck Regulator

Refer to schematic TRNT-EL-04-2001 page 6.

There is a further variation to the basic buck regulator design that is used to provide a cleaner and adjustable power supply to supply the analog power supply group. Adjustment of these supplies is required since reduction of the consumption of energy and generation of heat is accomplished by tuning the analog voltage rails to supply the optimum potential to the AFE boards. Using the VCB supply rails as an example, if clock rails (or biases) must generate that swing between +15v and –15V then VCB power supply potentials of +/-18V must be generated. The dissipation of the amplifiers on the AFE board should be expected. However, if only clocks (and biases) are required to swing between +12v and –8v for example, then tuning the VCB+ supply to +15v and the VCB- supply to –11v will allow conservation of approximately 3 Watts of power (and heat) dissipation.

In the VANA+ regulator the ouput of the basic switching regulator is fed to a low dropout series regulator (U7) to remove the switch mode supply ripple and attenuate any conducted EMI. The reference voltage for this device is generated first by the set current flowing out of U7 pin 4 (@10 μA) that produces 10v across R25, and secondly by the zener shunt of D17 (5.1v) to the output of the

amplifier U32:A. This means that the set voltage at U7 pin 4 will always be 5.1v above the output of U32:A. This establishes the lower limit of adjustment to be 5v. U32 is a simple non-inverting gain of three amplifier that multiplies the voltage seen across C102. This voltage is generated by a pulse width modulated signal generated by the Virtex FPGA on the LCB. The driver on the LCB that supplies this signal to the PSM is a 3.3v CMOS output which is divided and filtered by R9/R12/C102 to provide a dc value of between 0.1v and 2.5v. This value, multiplied by the gain of U32:A means that the set voltage on U7 pin 4 will vary between approx. 5.2v and 12.7v. This set voltage is used as the reference for the regulation of the output voltage VANA+.

In the adjustable regulator version the switchmode regulator control is now taken from the output of the series regulator (U7) by setting the gate voltage of the P-Channel MOSFET Q2 at the regulated output via R111. This MOSFET has a gate threshold of approximately -2v and shunts the feedback voltage divider resistor R107 to a value that is 2v lower than the output value of U7. The switchmode regulator therefore drives the inductor L2 harder to preserve a positive 2v headroom between the output L2 and the output of U7. This is sufficient to maintain regulation in the linear regulator while minimizing the dissipation of U7 and provide enough headroom to increase the output of U7 if the amplifier (U32) demands it.

2.10 VCB+ Positive Buck Regulator

Refer to schematic TRNT-EL-04-2001 page 7.

This regulator is similar to the VANA+ regulator described previously with an amplifier (U32:B) gain of 4 and a zener diode (D3) value of 9.1v to set the lower limit of the output voltage. In all other respects this regulator is the same as the VANA+ regulator.

2.11 VANA- Negative Inverting Buck Regulator

Refer to schematic TRNT-EL-04-2001 page 8.

This regulator employs the same topology as the positive regulator (VANA+) but the output of the primary inductor (L9) is now tied to GND. This forces the energy stored in the inductor during the on period to pass through D31 and force the PGND terminals negative. This produces a negative output voltage at the PGND pins and provides the negative reference for the switching regulator so all control functions and feedback paths are referenced to the negative rail in this design.

The input capacitors (C138, C143, C149) are wired to steer the ‘on-time’ current directly through the capacitors without having to pass through the output capacitors to reach ‘ground’. This means that they are operating with the sum of the primary power potential and the negative potential across them, that is, up to 36v.

The analog switches (U26, U28) are wired to accommodate the negative potential in these regulators by taking their negative supply pins to the regulator negative rail voltage. This provides a level shifting function and allows a common interface with the positive regulators.

The internal VCC voltage for U25 (pin 1) is referenced to the AGND (pin10) of the device. When the regulator goes active, pin 10 drives to the full negative potential of the supply. When this pin reaches approximately 7 volts, Q18 will begin to conduct and supply a lower potential than the VIN pins (3,4) to provide the internal regulator. This will reduce the internal regulator dissipation in the same way as the positive regulators.

The negative LDO device (U44) uses a different part to provide the regulated negative regulator and a different scheme to supply the set voltage. The amplifier (U42) works in the positive potential domain to provide the ground reference for U44 setting resistor R159. When the PWM adjustment signal from the FPGA is at or near zero volts, the R161 provides a value of –3.8v at pin 4 referenced to U42 pin 1 with the regulator output at –10v. By applying a positive offset on the output of U42:A, the output of U44 tracks positive to maintain the 3.8v potential across R161. In this way the regulator U44 adjusts its output on pin 3 with a 1:1 ratio to the output of the amplifier U42:A pin 1.

Because the adjustment control range is inverse, that is, a positive offset produced by the amplifier is less potential on the negative supply, the PWM signal produced by the FPGA to control the negative regulators is inverted in firmware i.e. 100% indicated PWM equates to the output of U42:A being near zero.

2.12 VCB- Negative Inverting Buck Regulator

Refer to schematic TRNT-EL-04-2001, page 9.

This regulator is a copy of the VANA design with modified gain on U42:B and a different LDO regulator sense voltage divider formed with R135/R133.

2.13 VHV Push Pull Regulator

Refer to schematic TRNT-EL-04-2001, page 10.

The VHV regulator is special because it has to step up the primary power source to achieve a nominal 35 volt potential. This allows the supply to be isolated from the primary power source by a transformer (T1) to reduce noise contamination from the primary source to the supply, and to allow the output of this regulator to be configured to supply either +30v / -5v or +5v / –30v supply to accommodate N-Channel and P-Channel detector technology. Selecting and connecting the required center tap of the transformer to the power supply ground via relay K1 contacts achieve this while providing a lower voltage potential on the opposing polarity to provide head room for the bias amplifiers on the AFE board.

The regulator is shown as a push-pull PWM step-up topology using a Linear Devices LT1533 device (U13) especially suitable for low noise power supply generation. This controller uses voltage and current sensing to modify the edge rate of the internal transistor switches. This considerably reduces the production of high frequency spurs (at a moderate reduction in efficiency). Unfortunately this device is not directly compatible with the primary power source potential and requires Q12 and Q13 to form a cascode pair that buffers the internal switching transistors against the higher voltage seen in the primary of T1. The switching waveform seen by the regulator's internal transistor collectors (pins 2, 15) are run at the VIN voltage of 6.8v set by local regulator Q14. The VHV regulator is not adjustable and produces a voltage programmed by the two pairs of resistors R131/R132 for positive voltage and R45/R48 for negative voltages. Regulation uses the feedback input with the absolute highest potential.

Heavy inductive and capacitive filtering (L10, L11, L13, L14 and C30, C41, C42, C50, C51, C113) is used at the output to remove as much of the switching ripple as possible. These voltages are post-regulated on the analog front end boards to further reduce ripple at theh high voltage bias amplifiers.

Q6 selects in which polarity the circuit works. When the gate of Q6 is low the VHV generator produces a negative high voltage supply for use with P-Channel detectors.

2.14 Auxiliary Circuits

Refer to schematic TRNT-EL-04-2001, page 11.

Each physical circuit board in the Torrent DHE is required to present a standard I2C interface with predefined devices to enable unique board identification and system calibration processes to be carried out. These devices are U22 and U36 that provide local temperature telemetry of the PSM, U46 which is a small serial eeprom used to store calibration constants for the PSM and U21 which is a unique silicon serial number device.

The presence of an I2C bus indicates that the hardware module is present and can be used. The presence test requires that there be three wires associated with the I2C bus. These are a standard serial clock used for synchronous data transmission called SCLK, a data input or source wire called SDA_SRC, and a data output or sense wire called SDA_SNS. The SDA_SRC and SDA_SNS wires are connected on the interface via an 825 Ohm resistor. The Virtex FPGA on the LCB uses this connectivity to allow it to poll the interface and establish presence. This connectivity scheme also allows the use of a remote power source, SDA_SRC pulled high, for the pull up resistor (R151) when data is transmitted from a slave device to the FPGA I2C master controller. The standard devices and their logical addresses are listed in Table 5.

Table 5 - Standard I2C Bus Device Assignments

Circuit Designation	Device	Purpose	Interface Address
U21	DS28CM00	Silicon serial number to uniquely identify the hardware. Telemetry shows this as tsmSiliconSerialNum.	0x50
U46	24AA128	4096 x 32-bit EEPROM to store detector coefficients and system identification with the detector dewar.	0x54
U22	MCP9803	Local temperature sensor for DHE monitoring. Telemetry shows this as tsmTemperature1.	0x48
U36	MCP9803	Local temperature sensor for DHE monitoring. Telemetry shows this as tsmTemperature2.	0x49

U23 and U43 provide a standard optoisolated interface for control of a shutter and preflash command. These devices are driven directly from the 3.3v logic buffer on the LCB.

U24 and U45 provide a means of communicating shutter status to the DHE via a standard optoisolated interface. Each pin of these devices is brought out to the application to allow easy positive or negative logic shutter status signals to be interfaced. Shutter state is defined in Table 6.

Table 6 - Shutter Status Coding

SENSE_OPEN	SENSE_CLOSE	Shutter Status
FALSE	FALSE	Shutter is opening or disconnected
FALSE	TRUE	Shutter is fully closed
TRUE	FALSE	Shutter is fully open
TRUE	TRUE	Shutter fault

2.15 VBB Push-Pull Regulator

Refer to schematic TRNT-EL-04-2001, page 12.

The VBB regulator is designed to supply the back side bias potential requirements used in deep depletion detectors. The regulator consists of two parts, the voltage generator and the low noise regulator. The voltage generator is of the same design as the VHV regulators with a different transformer, with the secondaries wired across a full bridge rectifier. Local feedback regulates the circuit to produce 70v across the output of the bridge formed by D9, D10, D26 and D27.

The high voltage potential is switched to provide a polarity complimentary to the selected VHV mode (P-Channel or N-Channel detectors) by grounding one side of the rectified output through K1.

The resulting ground referenced potential is applied to amplifier U47:A, which uses a standard feedback topology using R172/R176 for a gain of 2 and a positive feedback bootstrap topology (R93/R173) to achieve a total gain of approximately 10. The power supply for this amplifier is derived from Q7 and Q8, which provide up to 40v of potential across the amplifier centered on the voltage of the output on pin 7. This allows the regulator set reference voltage produced by U27:B to be inside the common mode range of U47 at all times. The set reference voltage, which appears on pin 7 of U27:B, is generated in the standard way by amplifying an integrated version of the PWM signal supplied by the FPGA, which appears on C93 after scaling by R96/R97. Amplifier U27:B provides a positive output voltage when the VHV_POL_SLCT signal is low and a negative output when this signal is high by filtering this signal to provide an inverting feedback offset voltage.

The networks of C87, C139, C140, C147, C148 is used to maintain the stability of U47 and limit the slew rate of the VBB regulated supply. When using this supply a separate ground reference is provided by the VBB_RTN path to allow a detector reference pin (guard pin) to be directly connected to this supply without passing through the Analog Front End boards.

2.16 VHTR Current Regulator

Refer to schematic TRNT-EL-04-2001, page 13.

This regulator uses a buck / boost mode LED controller device (U10)from Linear Technology to control a current passing through a heater resistor mounted adjacent to the detector in the Dewar. This heater is used to stabilize the detector temperature. The controller is operated in the buck mode and sinks current from the raw 24v supply. The heater current is sensed by the 0.2 Ohm resistor (R123) and used in the feedback loop to compare against the demand established by the **VHTR_ADJ** signal that is integrated by C36 to produce a DC value. This is the same principle as all the other circuits. A PWM signal is generated to provide the control voltage to the controller.

The maximum heater current can be limited by a choosing a value for the resistive divider formed from a resistor on the TSM-UTIL board and R122. This provides a hardware safety limit that is set on each transition board depending on the particular heater configuration. Current limit range should be from 3 to 10 watts. The maximum current that can be sunk by the controller is 500ma. The fuse (F1) protects the obviously dangerous heater positive supply and allows a convenient place to measure the current when calibrating the current measurement system.

The circuit includes electronics to measure the actual heater voltage potential (U11, U14) and the heater current (U9, U8). These values are sensed by instrumentation amplifiers and used to generate two variable frequency pulse streams. These pulse streams are used by the LCB to calculate and

control the heater circuit in closed loop with one of the selected temperature sensors near the detector acting as the feedback.

Q4 is only biased on when the heater is enabled to protect the primary power supply. There is provision to suspend the heater supply when a detector readout is in progress should this signal prove to add noise to the video signal.

The small regulator represented by U48 produes a low current 12v potential that is used for biasing the amplifiers and analog switches used in the PSM design. It is also made available to the TSM-UTIL board to power the temperature sense circuits. This supply is always enabled whenever the DHE has power applied.

2.17 Local Control Board Connector

Refer to schematic TRNT-EL-04-2001, page 14.

Connector **J1** carries the power supply voltages to the Local Control Board (LCB) of the DHE. The supplies are listed in Table 7. The power supply connector is a **SAMTEC LS2–130–01–S–D** type. This connector also carries the power supply control signals generated on the LCB and used to control the PSM. The power supply control signals are digitally generated at 3.3v logic levels from buffers on the LCB and are of three types: Binary levels, pulse and pulse width modulated. Table 8 describes these signals.

Table 7 - J1 Power Supply Voltages

Supply Name	Pins	Polarity	Voltage	Purpose
VCC	1,3	Positive	3.3v +/-10%	Digital logic supply to the LCB
VFAN	59	Positive	+7 to +14	Fan supply for DHE Temeperature control
VANA+	53,55	Positive	+5 to +10	Video processor circuitry supply voltage
VANA-	35,37	Negative	-10 to -5	Video processor circuitry supply voltage
VCB+	49,51	Positive	+9 to +18	Clock and low voltage bias supply voltage
VCB-	39,41	Negative	-18 to -9	Clock and low voltage bias supply voltage
VHV+	47	Positive	+30 or +5 +/-10%	High voltage bias supply voltage
VHV-	43	Negative	-5 or -30 +/-10%	High voltage bias supply voltage

Table 8 - J1 Power Supply Control Signals

Signal Name	Pin	Polarity	Type	Purpose
VCC_SYNC	5	Neg Edge	Pulse	Synchronizes the VCC, VFAN, and VHTR switching reg frequency
LCB_SHUTTER	6	Positive	Level	True turns on the open collector of the shutter optocoupler to control the instrument shutter.
VBB_ENABLE	11	Positive	Level	Enables the generation of the VBB supply voltage
VBB_ADJ	12	Both	PWM	Adjusts the voltage of the VBB supply between 0 and 65v
LCB_PREFLASH	13	Positive	Level	True turns on the open collector of the preflash optocoupler to control a flat field light source.
LCB_PWR_KILL	14	Negative	Level	Shuts down the VCC voltage regulator using the switch controller.
LCB_PWR_INT	15	Negative	Level	Signals the LCB that a user power supply shutdown is requested when the push button is activated.
VANA_SYNC	20	Neg Edge	Pulse	Synchronizes the +/-VANA switching reg frequency
VANA_ENBL	21	Positive	Level	Enables the generation of the +/-VANA supply voltage
VCB_ENBL	22	Positive	Level	Enables the generation of the +/-VCB and +/-VHV supply voltage
VCB_SYNC	23	Neg Edge	Pulse	Synchronizes the +/-VCB switching reg frequency
/VHTR_SUSPEND	24	Negative	Level	Suspends the VHTR switching regulator during detector readout if it causes noise problems.
VHTR_ENBL	25	Positive	Level	Enables the generation of the VHTR supply current
VHTR_ADJ	28	Positive	PWM	Adjusts the current of the detector VHTR supply between 0 and 500ma.
VANA+_ADJ	31	Positive	PWM	Adjusts the voltage of the VANA+ supply between +5 and +12v
VCB+_ADJ	32	Positive	PWM	Adjusts the voltage of the VCB+ supply between +9 and +18v
VCB-_ADJ	33	Negative	PWM	Adjusts the voltage of the VCB- supply between -9 and -18v
VANA-_ADJ	36	Negative	PWM	Adjusts the voltage of the VCB- supply between -5 and -12v
VHV_POL_SLCT	45	Positive	Level	True selects +30/-5v HV supply voltages and a negative VBB voltage. False selects +5/-30v HV supply voltages and a positive VBB voltage.
VHV_SYNC	46	Positive	Pulse	Synchronizes the +/-VHV and VBB switching reg frequency
VFAN_ADJ	57	Positive	PWM	Adjusts the voltage of the VFAN supply between +7 and +14v for DHE temperature stabilization
VFAN_ENBL	58	Positive	Level	Enables the generation of the VFAN supply voltage

J1 also corries several status and data signals to and from the LCB. This signal group employs level, pulse and I2C signalling protocols. These signals are listed in Table 9.

Table 9 - J1 Status and Data Signals to the LCB

Signal Name	Pin	Polarity	Type	Purpose
/LCB_SHUTTER_CLOSED	7	Negative	Level	Shutter is closed status input. True when U43 LED is on
/LCB_SHUTTER_OPEN	8	Negative	Level	Shutter is open status input. True when U42 LED is on
TEMP_1	9	Positive	Pulse	Detector temperature sensor 1. Open Collector output to LCB. Pulse train calibrated to 500Hz/Deg. K.
TEMP_2	10	Positive	Pulse	Detector temperature sensor 2. Open Collector output to LCB. Pulse train calibrated to 500Hz/Deg. K.
HTR_CURRENT	16	Positive	Pulse	VHTR current telemetry. Open Collector output to LCB. Pulse train calibrated to 200KHz/Amp.
HTR_VOLTAGE	17	Positive	Pulse	VHTR voltage telemetry. Open Collector output to LCB. Pulse train calibrated to 8KHz/Volt
PSM_SDA_SRC	18	Negative	I2C	Power Supply I2C data path from the LCB to the local memory, temperature sensors, and silicon serial number devices.
TSM_SDA_SRC	19	Negative	I2C	Transition module I2C data path from the LCB to the TSM local memory, temperature sensors, silicon serial number devices, and presence indicator.
PSM_SCL_SRC	26	Positive	I2C	Power supply I2C data clock from the LCB to the PSM.
TSM_SCL_SRC	27	Positive	I2C	Transition module I2C data clock from the LCB to the TSM.
PSM_SDA_SNS	29	Negative	I2C	Power Supply I2C data path to the LCB to the local memory, temperature sensors, and silicon serial number devices.
TSM_SDA_SNS	30	Negative	I2C	Transition module I2C data path to the LCB from the TSM local memory, temperature sensors, and silicon serial number devices.

2.18 Transition Module Connector

Refer to schematic TRNT-EL-04-2001, page 14.

Connector **J2** carries power and signaling directly to the Transition Module (TSM) via a short cable and **P2**. The **J2** connector is a 26-pin 0.1" dual row header and the **P2** connector is a **CANNON DBSFY-25S-A191** type. There is a cryostat heater supply and provision for two temperature inputs from the TSM-UTIL board. There are also control lines for controlling and sensing an electromechanical shutter and control of a 'Preflash' function.

In addition, the I2C interface signals from the Local Control Board (LCB) pass directly through the PSM to this connector to allow the LCB to sense the Transition Module presence and read a parameter file stored in I2C EEPROM memory on the TSM without requiring the physical presence or the powering up of an Analog Front End board (AFE). The signals are detailed in Table 10.

Table 10 - J2 Transition Module Connector Signals

Signal Name	Pins	In/Out	Type	Purpose
INPWR_SHLD	1	⇔	GND	Independent shield connection to chassis gnd
TSM_SCL_SRC	2	Out	I2C	Transition module I2C data clock from the LCB to the TSM.
PREFLASH_ON	3	Out	Level	Open collector output for preflash source control. Max 60v @ 50ma. Emitter is pin 7.
TSM_SDA_SRC	4	Out	I2C	Transition module I2C data path from the LCB to the TSM local memory, temperature sensors, silicon serial number devices, and presence indicator.
SHUTTER_OPEN	5	Out	Level	Open collector output for shutter control. Max 60v @ 50ma. Emitter is pin 7.
TSM_SDA_SNS	6	In	I2C	Transition module I2C data path to the LCB from the TSM local memory, temperature sensors, and silicon serial number devices.
SHUTTER_RTN	7			Common emitter for preflash and shutter control signals.
VHTR_LIMIT_N, P	8,10	In	Analog	Sets the maximum vhtr current limit via a resistor between these pins.
SHUTTER_SENSE_ OPEN_P, N	9,11	In	Level	LED of optoisolator for shutter open status input
VHTR_P	12,14	Out	Power	Fused vhtr positive rail at approx. 22v
SHUTTER_SENSE_ CLOSE_P, N	13,15	In	Level	LED of optoisolator for shutter closed status input
VHTR_N	16,18	Out	Power	Controlled leg of vhtr current regulator.
TEMP_1	17	In	Pulse	Open collector output of detector temperature value from sensor 1. 500Hz / Deg K
TEMP_2	19	In	Pulse	Open collector output of detector temperature value from sensor 2. 500Hz / Deg K
GND	20,22		GND	Power ground for tsm-util circuits
GNDE	21		GND	Chassis ground pass through to TSM.
VBB_SRC	23	Out	Power	Detector back side bias supply
VBB_RTN	24		GND	Detector back side bias supply return
VP12	25	Out	Power	tsm-util power supply. 12v @ 60ma.

3.0 Local Control Board (LCB)

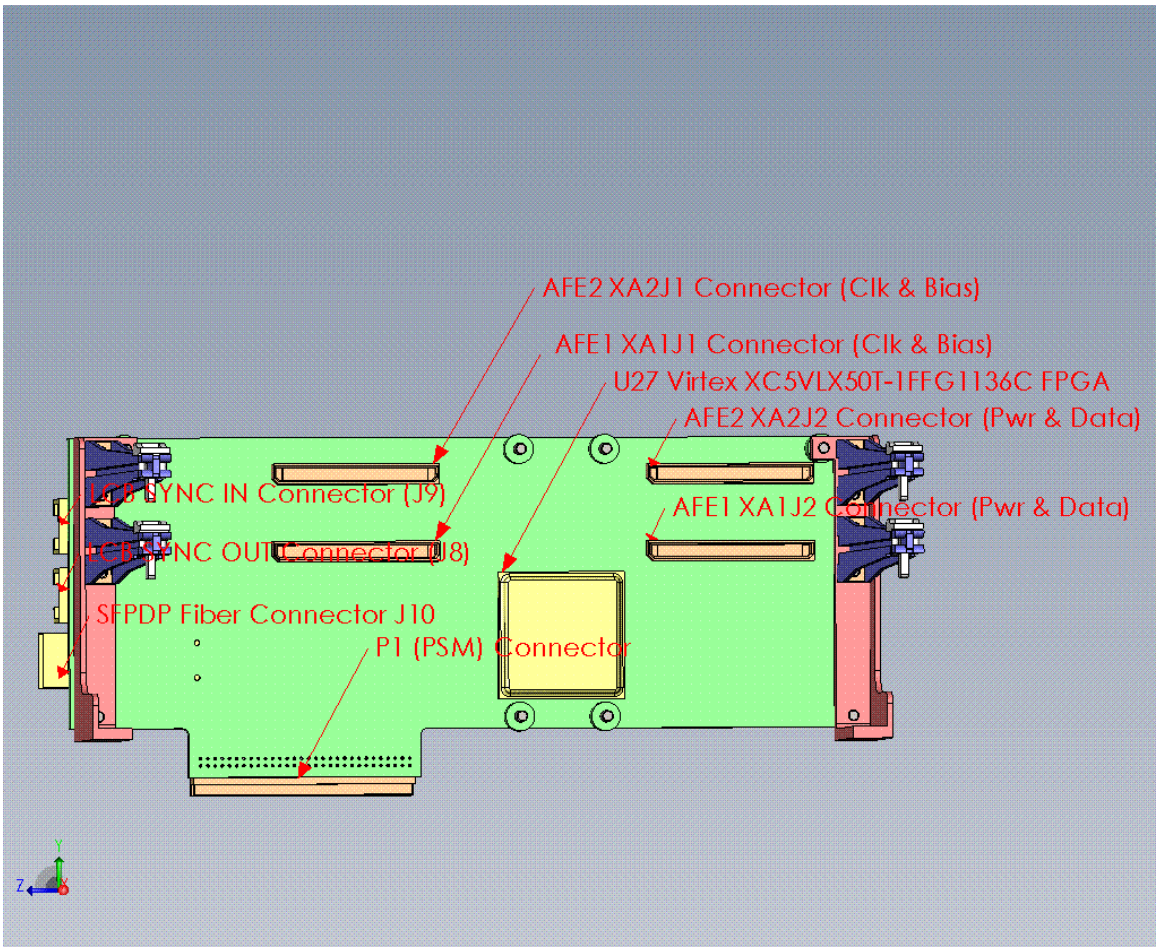
Refer to schematic TRNT-EL-04-2002.

This description corresponds to Revision –B– of the hardware.

3.1 Purpose of the LCB

With the exception of a small amount of interface logic located on the AFE boards, the LCB contains all of the digital logic required for the controller module functions. The LCB plugs directly into the power supply and forms an active backplane to support the AFE boards. Figure 3 shows the physical aspect of the front of the board.

Figure 4 - Local Control Board



3.2 Virtex 5 FPGA Characteristics

The major portion of the logic design is encapsulated inside one Virtex 5 FPGA made by Xilinx Corporation. The Xilinx device part code is XC5VLXT-1FF1136C. This device is based on a fabric of programmable logic blocks called Configurable Logic Blocks (CLBs) and specific function hardware blocks. These elements are interconnected and programmed during the power-on sequence by a eeprom storage elemnt. After programming the CLBs adopt functional behavior that determines the characteristics of the controller itself, that is, what the controller can do and how it does it. The FPGA programming is volatile and requires a new programming cycle each time power is applied.

Programming is normally done automatically from an eeprom memory (U43), however, there is a provision to program the device from a JTAG port (J3) as an alternative during code development.

When reading the schematic diagrams for the LCB you will see that this device, with over one thousand pins, is seen as separate symbols on each page. This has been done to separate the multitude of FPGA I/O pins into something approaching logical groups so functional relationships are clear between the portions of the FPGA and other PCB components.

The FPGA has fifteen banks of I/O. Each bank can be configured for a class of I/O functions based on the electrical characteristics required by other devices. Much of the logic is driven at 2.5v and 3.3v CMOS levels (LVCMOS25, LVCMOS33). Most clock sources are driven as either 2.5v differential voltage or differential current signals (LVDS_25, LVPECL_25). The image memory is interfaced using a controlled impedance Stub Series Terminated interface signal plan (SSTL18_II). These different interface standards use different power supply levels (2.5v, 3.3v or 1.8v) so each bank of the FPGA has a specific I/O power supply associated with it. The appropriate interface standard for each bank of the FPGA inputs and outputs can be found by looking at the VCC_xx pins on each section of the FPGA symbol. These pins supply the I/O potential to the FPGA for individual sections of logic.

In addition, the core logic operating voltage for the FPGA requires a 1.0v power supply, the gigabit transceivers require a clean 1.2v supply, and the FPGA auxilliary finctions require a 2.5v supply. These power supplies are generated locally on the LCB from the 3.3v supply (U9, U20, U56, U83) to satisfy the FPGA power supply requirements. The image buffer memory requires a 1.8v and 0.9v supply generated by U37 and U50. More information on the Virtex FPGA device can be found here and by searching the Xilinx web site here.

3.3 Clock Generator, Sync Ports and Reset

Refer to schematic TRNT-EL-04-2002 page 1.

Generally all logic performed on the LCB is synchronous to a clock. The principle clock source for the LCB originates at Y1, a 106.25MHz oscillator with a differential current (PECL) output stage (OCLK). This clock is divided by two and fed to a 2:1 multiplexor internally to the FPGA. The output of the multiplexor sources the BCLK and synchronizes all logic driven by SYSCLK internal to the FPGA logic. This 2:1 multiplexor is used to commute the clock source when the DHE is run as a slave device. This is configured by setting the DHE_IS_SLAVE attribute true and upon detection of the SYNC_CLK_IN clock source. Under these conditions the OCLK is switched off (by Q2) and the SYNC_CLK_IN source is used to drive BCLK and the internal logic via SYSCLK. This allows several Torrent DHE units to be run together to control a single focal plane without causing interference to each other.

The BCLK output from the FPGA is fed to a programmable clock synthesizer (U28). This device contains a phase lock loop and divider networks to allow six other clock sources to be generated. These clocks are listed in Table 11.

Table 11 - LCB Clock Sources

CLK Name	FPGA In/Out	Freq. MHz	Usage
OCLK	IN	106.5	Primary clock source when DHE is a Master
BCLK	OUT	53.125	Synchronization source for U28
SYNC_IN_CLK	IN	53.125	Primary clock source when DHE is a Slave
SYNC_OUT_CLK		53.125	Source clock for DHE Slave when this DHE is a Master
LCLK	IN	53.125	Serial FPDP comm. port data clock to Virtex GPT
TCLK	IN	39.8484	ADC data clock
MCLK	IN		Not used – Spare – Disabled.
DCLK	IN	79.6875	AFE Gateway interface clock
PCLK	IN	159.375	Image memory interface clock
SYNC_CLK_SNS	IN	53.125	Sync port data clock when DHE is a Master
SYNC_CLK_SRC	OUT	53.125	Alternate Sync port data clock. Not used

The clock synthesizer device (U28) is programmed by the firmware to generate these clocks during the power on sequence using a simple serial protocol employing signals **CLK_CTRL_CLK**, **CLK_CTRL_DATA** and **/CLK_CTRL_CS**. The signal **CLK_CTRL_SYNC** is used to align the clock edges when pulsed at the end of the programming operation. Signal **CLK_CTRL_GOE** is then sent true to enable the clock synthesizer outputs. The signal **CLK_LOOP_LOCK** can be tested on TP9 and should be a true signal when the clocks are being synthesized correctly. The voltage on pin CP and TP7 is the steering voltage for the synthesizer VCO and should be approximately 1.6v with low ripple when the PLL is locked.

The sync clocks together with sync data and sync strobe signals are used for communication and synchronization between separate Torrent DHE modules when used together to control a single focal plane. This is desirable to minimize interference between the DHEs that may cause noise on the detector video signals.

Up to four DHEs may be daisy chained to form a ring topology by connecting a standard (non-xover) RJ54 network cable between the LCB_SYNC_OUT port (J8) to the next DHE's LCB_SYNC_IN port (J9) and continuing this hook up scheme until the last DHE is connected back to the first DHE. In this configuration any of the DHEs may be assigned as the DHE Master via software.

Only one Master is allowed on the loop. The Master DHE then supplies the Slave DHEs with a clock source via OUTSYNC_CLK that propagates through the ring with a certain propagation delay. This delay is measured by the DHE assigned as master and a compensation made for each DHE Slave in the group to allow synchronization to be achieved within a half clock cycle of the Master clock source, that is, within 9ns.

Sync signals that are sourced and received by the DHE use a differential LVDS interface to maintain ground isolation between the individual DHEs. This scheme works when the ground potentials between different DHE modules is within the common mode range of the LVDS transmitters (U55, U78, U79, U81) and the receivers (U75, U76, U77, U80), which is between 0.6v and 2.6v. Transmitters are DC coupled to the outputs whereas all receiver inputs are AC coupled to block any DC current flow.

Inputs and outputs also have ESD protection devices. U1, U2, U3 and U4 act as these protection devices.

There is a provision to set equalization values for the individual links that provides compensation for cable characteristics to minimize signal distortion. These signals can be configured using software to set appropriate attribute values.

All serial data transmissions (OUTSYNC_OUT, OUTSYNC_IN, INSYNC_IN, INSYNC_OUT) and the synchronization pulses (OUTSYNC_STB, INSYNC_STB) are synchronous to the link clocks (OUTSYNC_CLK, INSYNC_CLK). The serial data signals provide a short and moderately fast bi-directional data link between DHE modules.

This data link is used to establish the ring delay coefficients. The strobe signals are used to initiate sequencer operations so they are synchronous to the Master DHE.

3.4 LCB Reset functions

Reset switch SW1 provides a local method to hard reset the LCB by initiating a power-up sequence that reloads the FPGA from the eeprom store. This reset is also asserted during power-up by the RC pair R116/C6. The monostable U70 provides a shaped low true pulse (approx. 50µs) to the PROGRAM pin of the LCB via Q1, which initiates the hard reset cycle. A hard reset can also be initiated by software control by setting an appropriate attribute. This causes the signal **/REBOOT** to be asserted low, which initiates a pulse from U70:B.

The other half of U70 is used as a watchdog timer that is set by a stream of pulses initiated by a timer running off the SYSCLK source in the FPGA. This means that under normal operation U70 pin 4 is high true. If the primary clock source should be lost because the DHE is running in slave mode and the SYNC_IN cable becomes defective or disconnected, U70 pin 4 goes low that initiates a hard reset.

The signal **/WATCHDOG_FAIL** is routed directly to the AFE boards and immediately disables the clock and bias outputs to protect the detector should a clock failure occur.

3.5 JTAG and FPGA Configuration

Refer to schematic TRNT-EL-04-2002 page 2.

The configuration process of the FPGA occurs whenever power is applied or a hard reset occurs. In either of these cases the signal **/PROG_B** is asserted low and that causes the FPGA to go into a configuration sequence. After this signal returns high, the FPGA enables a configuration clock on signal CCLK and sequences the signals **DONE, /INIT_B**, and **/PROG_B** to condition the configuration eeprom store, which is device U43. The configuration data stream is carried on signals **CFG_DATA[0:7]** while the start address of the data comes from the state of signal **AFE_SCL_SRC0**. This address option enables different configurations to be loaded for the IR or CCD versions of firmware for the DHE. The configuration process takes approximately 40ms. After loading the configuration

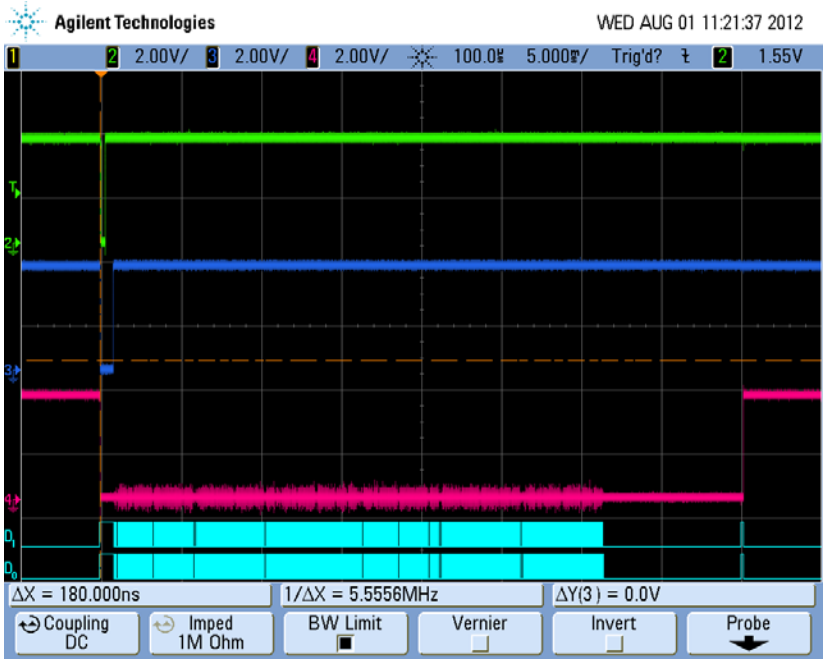
data, the FPGA sequences the process of internally enabling I/O outputs, locking DLLs, and so forth. More information on the FPGA configuration process can be found here.

The configuration data contained in U43 is programmed via the JTAG interface using connector J3. This is easily accomplished by using the Xilinx Impact tool to load a compiled .mcs file to the eeprom. The The JTAG chain connects two devices to a suitable JTAG controller U43, which is a Xilinx XCF32P eeprom and the Virtex 5 FPGA device U27. JTAG communications use a 3.3v logic convention. The Virtex FPGA can be directly loaded with a configuration .bit file by the same means.

Once configuration has taken place the **CFG_DATA[0:7]** signals are used by the FPGA to supply a set of debug signals to connector J4. J4 signals must not have any significant load attached to them during configuration, however, the standard Agilent MSO signal pods do not affect configuration. The debug signals available at the J4 connector are described in the firmware description section of this manual.

Figure 5 shows the basic boot process timing.

Figure 5 - FPGA Boot process timing



Trace	Signal
Green	PROG_B (Q1 Drain)
Blue	INIT_B (TP4)
Red	DONE (TP5)
D1/D0	CFG_DATA(1:0)

3.6 Communication Ports

Refer to schematic TRNT-EL-04-2002 page 2.

There are a total of five communication ports that the LCB supports. Three of these are public in that they support standard industrial protocols. Table 12 lists these ports and their protocols.

Table 12 - LCB Communication Ports

Port Name	Conn.	Protocol	Bandwidth	Usage
SFPDP	J10	ICD 6.1 carried on Serial Front Data Port. Systran SL100 compatible.	1.0625Gbs.	Primary PAN command and pixel data stream communications port.
RS232	J12	Simple monitor on RS232.	9600,8,N,1	Debug port.
GIGe	J7	Simple monitor and raw pixel data carried on GigE Vision using Gigabit Ethernet via Pleora NTx-Mini interface	1.0625Gbs.	Secondary command and pixel data stream communication port.
SYNC_OUT	J8	Proprietary protocol	53.125Mbs	DHE to DHE downstream communications
SYNC_IN	J9	Proprietary protocol	53.125Mbs	DHE to DHE upstream communications

Serial Front Panel data Port (SFPDP) – Systran interface

The SFPDP communications utilizes one of the twelve available built in FPGA GTP gigabit transceiver to emulate the Systran SL100 protocol. This protocol is used to support the communications method between the PAN and DHE (ICD 6.1). The GTP transceiver requires a low jitter 53.125 MHz clock (LCLK) to synchronize the data bit rate using an FPGA internal DLL to produce a x20 data clock. The raw data transmitted from the FPGA port on signals SFP_TD+ and SFP_TD- is routed to J10 as a differential current pair (CML). J10 is a industrial standard connecter used to support the Small Form Factor Pluggable (SFP) transceiver modules. A Fiberxon FTM-8120C-LG optical transceiver is plugged into the SFP port to convert to 850nm optical signals compatible with the Systran module used in the PAN. Similarly the optical signals received by this transceiver from the PAN are converted to CML signals on the **SFP_RD+** and **SFP_RD-** signal pair. This signal is decoded by the GTP gigabit transceiver in the FPGA to produce a 32-bit FPDP interface internal to the FPGA.

Because of the high speed nature of these signals, the GTP section of the FPGA and the SFP port require significant filtering of power supplies to function correctly. This filtering is done by the various ferrite beads and capacitors associated with U27:H and J10.

The SFP standard provides a method for interrogating the SFP module to determine its characteristics using signals **SFP_MOD_DEF0,1,3**. These signals are not used in this implementation. However, the loss of carrier signal **(SFP_LOS)** and transmitter fault signal **(SFP_TXFAULT)** are monitored to assure correct port function. The **SFP_TX_EN** signal is used to power down the SFP transmitter when the port is disabled through software.

RS232 Interface

The RS232 port is driven by U54, which generates the correct bipolar voltages for the signals using a built in voltage generator using L8. The RS232 protocol is supported directly by the internal logic of the FPGA. The signals **UART_TX** and **UART_RX** signals carry the serial transmit and receive data stream at 3.3v levels. The **UART_PS** signal is used to shut down the voltage generator of U54 when the RS232 port is disabled through software.

The primary purpose for the RS232 port is to provide a last resort communication path for debugging or diagnosing the LCB board. Setting the appropriate software attribute in the LCB will allow all communications to and from the LCB (via a different port, such as the SFPDP) to be copied to the RS232 port so communications problems can be diagnosed.

This port supports a small monitor program that will interpret simple commands and allow the full range of control of the DHE as provided by ICD 6.1. The available commands, shown in Table 13, are prefixed with the 'plus' (+) character (0x2B) and completed with a Line Feed character (0x0A). The standard format of 9600 Baud, 8 bits, no parity is supported. Upper or lower case characters are recognized. All address and data values must be expressed in hex. Fields must be separated by a space or tab character. Backspace clears the current command, although currently the display looks messy.

Table 13 - RS232 Monitor Commands

1st Field	2nd Field	3rd Field	4th Field	Command
+A	16-bit Vector	Not Used	Not Used	Forces an Asynchronous Command to synchronize the communication channels after reset
+R	8-bit Module Number	16-bit Module Address	Not Used	Returns the 32-bit contents of the addressed register (in hex)
+W	8-bit Module Number	16-bit Module Address	32-bit Write Data	Writes the 32-bit value to the addressed register
+S	8-bit Start Vector	Not Used	Not Used	Triggers a 'Start Exposure' event in the sequencer with the 8-bit start vector

GIGe Interface

Refer to schematic TRNT-EL-04-2002, page 7.

The GIGe interface to the LCB is supported using an OEM module manufactured by Pleora Technologies Inc (more information here). The interface to this module is supported directly by the FPGA via connector J7. The module requires a 2.5v power supply provided by U84 that appears on J7 pins 1 and 2. There are two data transport sections on this interface. Raw pixel data is put onto the **VID_DAT[0:15]** synchronous to the **VID_CLK0** signal and validated by the high true **VID_DVAL** signal. Every time that this signal is true on the rising edge of the clock signal, pixel data is accepted on the video data signals and packaged to conform to the GIGe protocol. The **VID_CLK0** clock is provided by the FPGA at one half SYSCLK rate, that is, 26.5625 MHz.

The **VID_FVAL** signal is used to indicate the beginning of a new image frame. The **VID_LVAL** signal likewise indicates the first pixel of a new image line (row). These two signals are true for one pixel time. The GIGe interface is configured to use these signals as edge sensitive strobes. Together they

provide a method for an application using the GIGe interface to decode an image dimension without any prior information concerning the dimensions of the detector being read out.

The Pleora module also supports an 8-bit serial data link that is used to pass command and message data to and from an application using the GIGe interface. The serial interface is synchronous to a clock generated by the module on signal **SER_HB0_CLK**. The transmitter and receiver serial data streams are sent and received by the **SER_HB0_TX** and **SER_HB0_RX** signals respectively. The serial data is interpreted by the same small monitor as used on the RS232 port and shown in Table 13.

3.7 Image Memory

Refer to schematic TRNT-EL-04-2002, page 3.

The LCB has a small dynamic memory device (U31) that is used to buffer and descramble raw pixel data. U31 is a two gigabit storage device organized as 16-bit words by 128 megaword store divided into eight banks. The dynamic control of this device is managed entirely by the logic fabric of the FPGA. The memory functions as a two-port memory at a clock rate of 159.375MHz to store and recall pixel data at the DCLK rate of 79.6875 MHz, which is the pixel data transport rate. Resistor banks RN1, RN2, RN3 provide load termination to the VTT supply generated by U50. This regulator uses the memory power supply potential of nominally 1.8v to derive the required termination potential of half the supply value via the resistive divider R74/R75. All memory interface levels comply to SSTL18_II levels.

3.8 CCD AFE Digital Interface

Refer to schematic TRNT-EL-04-2002, page 4,5, and 6.

The digital interface to the AFE from the LCB is divided into three parts: The interface power supply, the clock and bias control signal group, and the data signal group. The interface to the AFE boards from the LCB is collectively known as the AFE Gateway.

The power supply for the gateway is designed to support the bi-directional voltage translation parts used in the interface (ON semiconductors, type NLSX3014). For each FPGA signal there is a bi-directional voltage translation device between the LCB and the AFE logic. This affords a clear isolation between the AFE interface power supply and the LCB interface power supply for noise immunity purposes. The translation devices are powered by a 2.5v supply potential on the LCB side and work at 2.5v LVCMOS signal levels from the LCB side.

The AFE side of the translation device is supported in normal use by a power supply potential generated on the AFE boards. The AFE side interface supply potential is nominally 3.3v but can be up to 4.5v. When the AFE is powered down a supply potential is still required by the translation devices on the AFE side and is supplied by the LCB 3.3v supply filtered by L2 and blocked by diode D1 (Page 6). This allows the translation devices to be within their operational specifications when the AFE is powered off and to assume the power supply of the AFE when these are powered up and the AFE supply is available. In this way there is a nominal 0.8v difference between the two sides of the translator power supply potentials that prevents noise transmission from the LCB to the AFE boards. The AFE interface power supply is designated as VPIFC and is seen on connectors XA1J1 and XA2J1 pins 1 and 2 (Page 6).

The clock and bias interface to the gateway uses the XA1J1 and XA2J1 connectors to connect eighty signals to both AFE boards (**AFE_CLKBIAS[0:79]**). These signals appear on the same connector pins on

both AFE board connectors and are defined entirely by the firmware and AFE hardware as to their usage. They can be assigned as inputs or outputs depending on the requirements of the AFE.

On the clock and bias signal group there are four groups of signals that are supplied that occupy different pins on the AFE connectors. These signals are **AFE_CLKBIAS[80:91]**. These signals are designed to be used as data strobes and/or clocks to the individual AFE boards. Table 14 explains the common and individual signals and their significance for the CCD AFE use on connectors XA1J1 and XA2J1.

This Table also shows the individual connection of the I2C data chain that supports the auxiliary circuits on the AFE boards. These signals are used to interrogate the I2C devices on the AFE board to provide calibration data, temperature telemetry and a unique serial number.

Table 14 - CCD AFE Gateway Clock and Bias Signals (Connectors XA1J1 / XA2J1)

LCB Signal Name	AFE1 Pins	AFE2 Pins	AFE CCD Signal Description
AFE_CLKBIAS[0:15]	[3:18]	[3:18]	Detector clock states
AFE_CLKBIAS[16:17]	[19:20]	[19:20]	Latched on AFE but not used
AFE_CLKBIAS[18:22]	[21:25]	[21:25]	Detector clock signal enables
AFE_CLKBIAS[23:31]	[26:34]	[26:34]	Test point control
AFE_CLKBIAS[32:47]	[35:50]	[35:50]	Not connected
AFE_CLKBIAS[48:56]	[51:59]	[51:59]	Bias and Clock DAC control
AFE_CLKBIAS[57:59]	[60:62]	[60:62]	Telemetry control
AFE_CLKBIAS[60]	63	63	Latched on AFE but not used
AFE_CLKBIAS[61:63]	[64:66]	[64:66]	Telemetry control
AFE_CLKBIAS[64:67]	[67:70]	[67:70]	Detector bias voltage enables
AFE_CLKBIAS[68:76]	[71:79]	[71:79]	DAC clear and reset signals
AFE_CLKBIAS[77]	80	80	DAC serial data clock
AFE_CLKBIAS[78]	81	81	Telemetry serial data clock
AFE_CLKBIAS[79]	82	82	Latched on AFE but not used
AFE_CLKBIAS[80]	83	84	AFE1 Interface Enable
AFE_CLKBIAS[81]	84	83	AFE2 Interface Enable
AFE_CLKBIAS[82]	85	86	AFE1 Write Clock Data Strobe
AFE_CLKBIAS[83]	86	85	AFE2 Write Clock Data Strobe
AFE_CLKBIAS[84]	87	88	AFE1 Spare Data In
AFE_CLKBIAS[85]	88	90	Not used
AFE_CLKBIAS[86]	89	87	AFE1 Write Utility Data Strobe / AFE2 Spare Data In *
AFE_CLKBIAS[87]	90	89	AFE2 Write Utility Data Strobe
AFE_CLKBIAS[88]	91	92	AFE1 Spare Data Out
AFE_CLKBIAS[89]	93	94	Not used
AFE_CLKBIAS[90]	92	91	Not used
AFE_CLKBIAS[91]	94	93	Not used
AFE_SDA_SRC0	95	96	AFE1 I2C serial data source
AFE_SDA_SRC1	96	95	AFE2 I2C serial data source
AFE_SDA_SNS0	97	98	AFE1 I2C serial data sense
AFE_SDA_SNS1	98	97	AFE2 I2C serial data sense
AFE_SCL_SRC0	99	100	AFE1 I2C serial data clock source

AFE_SCL_SRC1	100	99	AFE2 I2C serial data clock source

* This is a wiring mistake. However, it doesn't interfere with normal operation but does disallow the use of the AFE2 Spare Data In signal.

The **AFE_CLKBIAS[80:91]** signals are designed to be used as individual strobes to the two AFE boards so that independent control of each board can be realized. The firmware component uses several configuration attributes to allow the two AFE boards to be used independently or slaved to each other for identical response. As an example, depending on the setting of these configuration attributes, the DHE will provide either thirty two independent clocks or sixteen pairs of duplicate clocks to the detectors. In the first case the **AFE_CLKBIAS[0:15]** signals will be multiplexed with the **AFE_CLKBIAS[82:83]** strobes independently and the latter case both strobes will go true together to drive the data on the **AFE_CLKBIAS[0:15]** signals to both AFE boards simultaneously.

Bias and clock voltage adjustment is provided on the CCD AFE board by several DAC multichannel devices (AD5391). These devices are controlled through a simple Serial Peripheral Interface (SPI) using signals **AFE_CLKBIAS[48:56]**. The serial data **(AFE_CLKBIAS[48])** and synchronous serial data clock **(AFE_CLKBIAS[77])** are transported through the AFE board latch interface using the AFE Write Utility Data Strobe signals **(AFE_CLKBIAS[86,87])**.

Telemetry control to each AFE board is provided by signals **AFE_CLKBIAS[61:63]**. The telemetry interface is also controlled by SPI protocols and is synchronous to **AFE_CLKBIAS[78]**.

The arrangement of the AFE Clock and Bias interface combined with the FPGA Gateway allows synchronous control of both AFE boards so that the edges of the digital signals have a predetermined noise spectrum. This fact is used to minimize interference to the video processing circuits.

The data group signals on the gateway are routed via connectors XA1J2 and XA2J2 which also carry the power supplies to the AFE boards. These signals are also fed through the voltage translator devices and are defined entirely by the firmware and AFE hardware as to their usage. They can be assigned as inputs or outputs depending on the requirements of the AFE. The connector pin outs provide one common group and two distributed groups to provide individual connection between the LCB and the two AFE boards for data. The individual groups provide data paths to and from the AFE to the LCB. Table 15 shows the distribution of signals used on these connectors to support the CCD AFE boards.

Table 15 - CCD AFE Gateway Data Signals (Connectors XA1J2 / XA2J2)

LCB Signal Name	AFE1 Pins	AFE2 Pins	AFE CCD Signal Description
/WATCHDOG_FAIL	26	26	System fail detector signal shutoff
AFE_PWRDATA[0:17]	[27:61] Odd	[28:62] Even	AFE1 ADC serial data for 18 channels
AFE_PWRDATA[18:35]	[28:62] Even	[27:61] Odd	AFE2 ADC serial data for 18 channels
AFE_PWRDATA[36:43]	[63:70]	[63:70]	AFE Common CDS state signals
AFE_PWRDATA[44:47]	[71:77] Odd	[72:78] Even	AFE1 CDS Channels select signals
AFE_PWRDATA[48:51]	[79:85] Odd	[80:86] Even	Not Used
AFE_PWRDATA[52:55]	[72:78] Even	[71:77] Odd	AFE2 CDS Channels select signals
AFE_PWRDATA[56:59]	[80:86] Even	[79:85] Odd	Not Used
AFE_PWRDATA[60]	87	88	AFE1 ADC data clock
AFE_PWRDATA[61]	89	90	Not used
AFE_PWRDATA[62]	88	87	AFE2 ADC data clock
AFE_PWRDATA[63]	90	89	Not Used
AFE_PWRDATA[64]	91	92	AFE1 Data Interface latch strobe
AFE_PWRDATA[65]	93	94	Not used
AFE_PWRDATA[66]	92	91	AFE2 Data Interface latch strobe
AFE_PWRDATA[67]	94	93	Not used
AFE_PWRDATA[68]	95	96	AFE1 Data latch output enable
AFE_PWRDATA[69]	97	98	Not used
AFE_PWRDATA[70]	96	95	AFE1 Data latch output enable
AFE_PWRDATA[71]	98	97	Not used
AFE_PWRDATA[72]	99	100	AFE1 Write CDS state strobe
AFE_PWRDATA[73]	100	99	AFE2 Write CDS state strobe

Signals **AFE_PWRDATA[0:35]** are designed to be used as serial data paths from the CCD AFE ADC converters. This data is strobed out of the ADC components on the AFE board synchronous to the AFE ADC data clock signals **(AFE_PWRDATA[60,62])**. The ADC data is latched on each AFE Board by the two AFE Data Interface latch strobe signals **(AFE_PWRDATA[64,66])** and sampled by the FPGA through the Gateway interface at each bit time. This scheme allows up to a total of thirty-six channels of serial data to be acquired simultaneously (eighteen per AFE board). In the CCD AFE board case, only eight of these channels are utilized **(AFE_PWRDATA[0:3]** and **AFE_PWRDATA[18:21])**. In the CCD AFE case the signals **AFE_PWRDATA[4:17]** and **AFE_PWRDATA[22:35]** are used to transport telemetry data to the FPGA for monitoring of the AFE state. These telemetry signals are latched using the same AFE Data Interface latch strobe signals and sampled at a time interval by the Gateway interface.

The **WATCHDOG_FAIL** signal is used in conjunction with the separate clock and bias enable signals **(AFE_CLKBIAS[18:22]** and **AFE_CLKBIAS[64:67])** to connect the DHE electrically to the detector(s) that it is to control. Should the DHE lose the ability to control the detector(s) because of a loss of the primary clock source (mainly a risk when the DHE is running as a slave device) then the **WATCHDOG_FAIL** signal goes to a true (low) state to disconnect the detector from the DHE.

The **AFE_PWRDATA[36:43]** signals are used with the associated latching strobes **(AFE_PWRDATA[72:73])** to control the state of the Correlated Double Sampling (CDS) video signal processor logic on two CCD AFE boards. The CDS state information is driven either directly from the PAN by setting an attribute or from the DHE sequencer internal to the FPGA. The two sets of AFE CDS Channels select signals **(AFE_PWRDATA[44:47]** and **AFE_PWRDATA[52:55])** control which CDS circuits are commanded by the state information. This is mainly used to conserve power in video signal circuits that are not being used.

The two AFE Data latch output enable signals **(AFE_PWRDATA[68]** and **AFE_PWRDATA[70])** are used to enable the output of the AFE board data latches and are used when a parallel scheme of data transport is used by an AFE design. Under these conditions, each AFE board may send a thirty-six bit word on every other Gateway clock strobe. This scheme is not used in the CCD AFE and the latch output enable signals are always true after the AFE has been powered up.

3.9 LCB-MEZ Control

Refer to schematic TRNT-EL-04-2002, page 6.

All power supplied to the AFE boards is monitored by the LCB mezzanine board (LCB-MEZ). The LCB controls the enabling and monitoring of these supplies via connectors J5 and J6. The regulated power supplies generated by the PSM are routed on the LCB to J6 and supports the common ground reference point of the two AFE boards via pins on this connector that are directly routed back to the PSM ground pins. The LCB supplies a 2.5v potential on J6 pin 6 (AVDD) to bias the current sensing amplifiers on the mezzanine board for power monitoring.

Signals **AFE1/2_PWR_EN_VANA** and **AFE1/2_PWR_EN_VCB** on J6 and **AFE1/2_PWR_EN_VHV** on J5 are generated by the FPGA and control enabling the voltage groups to each AFE board. Only boards that are detected as present (via the I2C interface logic) are allowed to be enabled. A typical power sequence is to enable each AFE power group with a 50ms delay between them.

Signals on J6, pins 23:30 and J5 pins 9:12 are current monitor sense voltages representative of the consumption of each AFE board supply. These voltages are sent to the Virtex 5 FPGA System Monitor inputs on bank 13 of the FPGA I/O structure. The regulated supply potentials for the AFE are also monitored by this FPGA System Monitor function block connected to bank 13 via voltage dividers. See page 4 of the schematic. Negative PSM supplies are biased by a 1.0v reference to bring them into the dynamic range of the monitor function block.

Note that due to constraints on the number of telemetry ports available on the FPGA monitor block, only AFE1 has telemetry available for the VANA current monitor.

Four signals on J5 **(AFE1/2_PWR_FAIL_VANA**, **AFE1/2_PWR_FAIL_VCB**) are generated by over / under voltage conditions sensed on the mezzanine board. These signals are monitored by the FPGA to assure correct operation of the AFE boards.

J5 provides the separate power supply potentials to each AFE power and data connector (XA1J2 and XA2J2) as well as separated ground return paths. These power supplies are conditioned and protected to provide the correct operating voltages for the AFE boards.

3.10 I2C Interface

Refer to schematic TRNT-EL-04-2002, page 5.

One of the requirements of most Torrent circuit boards is the incorporation of an I2C bus that has four standard devices attached to it. This requirement allows the LCB to monitor the individual temperature of the boards, sense a uniquely identifying serial number for each board and provide a local memory to store unique hardware calibration characteristics.

The Virtex 5 FPGA firmware incorporates a single master, multi-slave interface to service five I2C busses. These interfaces are also used to indicate the physical presence of the boards and report back to the PAN the number of boards and the serial numbers present in any DHE. Page 5 of the schematic shows the interface to the two AFE boards that use U22, U23 and U24 to interface to the physical boards. The AFE I2C busses are powered from the VPIFC interface power supply so the AFE boards do not have to be powered up to detect them. An equivalent set of devices shown on page 7 (U14, U66, U67) are used to interface to the PSM and TSM I2C interfaces.

These four interfaces use a modified I2C topology in that the normally bi-directional serial data signal, SDA, is split into two signals, one that sources data to the I2C slave device **(xxx_SDA_SRC)** and one signal that acts as the sense for I2C slave devices serial data transmission **(xxx_SDA_SNS)**. On the slave interfaces of each board these two signals are bridged with an 825 Ohm resistor. By sensing the changes caused by changing the state of the source signals a conclusion can be reached as to the physical presence of the board without using the I2C protocol itself. This simplifies board presence test and allows the LCB to source the required serial data pull-up current for the data line through the series resistor by holding the source line high when expecting the slave to respond to a master request. This helps to control the return current path by maintaining separation between the boards' local power supplies and the LCB.

Page 7 of the schematic also show the I2C slave devices for the LCB module. U25, U26 and U57 form the local I2C devices that contain information about the LCB module. This I2C interface is classic because it uses just two wires to control the data flow between the I2C master (the FPGA) and the slave devices.

3.11 PSM Control

Refer to schematic TRNT-EL-04-2002, page 7.

The PSM requires a considerable number of signals to control the multiplicity of power supplies. Connector P1 connects these signals produced by the FPGA to the power supply. All signals are buffered by a normal non-inverting 3.3v CMOS buffer to provide some measure of protection to the FPGA and assure a strong drive capability. All of these signals have their functions explained in the PSM manual section.

There are two LED indicators mounted one each in the **SYNC_IN** and **SYNC_OUT** port connectors. These two LED indicators can be programmed through software attributes to indicate one or combinations of certain events that the DHE experiences. These indicators are normally extinguished but may be used for first line diagnostics at the instrument to indicate such things as pixel data flow, reset state, PAN communication flow, and so forth. The pull-ups on the two activation signals assure that the buffers are adequately biases since the LED control comes from a 2.5v I/O bank while the buffers are driven from the VCC 3.3v supply.

3.12 Local Power Supplies

Refer to schematic TRNT-EL-04-2002 page 7.

Device U20 and U37 are identical monolithic buck mode power supply regulators. These two devices supply the low impedance and highly stable power required to power the Virtex 5 FPGA core logic circuits at 1.0v and the image memory at 1.8v. Synchronization of these supplies is achieved via the square wave signal **LOGIC_SYNC** at a frequency between 720KHz and 1.56 MHz, synchronous to a multiple of the pixel conversion rate.

The 1.0v core voltage regulator will run whenever the 3.3v VCC power is available. The image memory power supply can be shut down using the appropriate software attribute that takes signal **MEM_PWR_EN LOW**. This signal is held high by R72 during the initial power up sequence since the FPGA boot eeprom also requires this supply during the power up process.

Signal **VAUX_EN** is used to enable the 2.5v linear regulator (U9) that regulates the AVDD supply used for the FPGA System Monitor. U83 supplies the bulk 2.5v supply used in the AFE interface logic design.

A single 1.0v reference supply is generated by the AVDD 2.5v supply to act as a reference for negative voltage sensing on the FPGA System Monitor inputs.

4.0 LCB Mezzanine (LCB-MEZ)

4.1 Introduction

Referenced to drawing TRNT-EL-04-2003.

This description corresponds to Revision –A4– of the hardware.

The mezzanine board provides power conditioning and monitoring functions for all analog voltage supplies used by the Analog Front End boards. These supplies are:

1. +/- VANA that is used to supply the video processing circuits and the interface logic supplies.
2. +/- VCB that is used to power the medium voltage bias and clock buffer amplifiers.
3. +/- VHV that is used to power the high voltage bias amplifiers.

The six supplies generated by the PSM are individually switched in pairs to each Analog Front End (AFE) board via voltage and overcurrent protection circuits. Connector P1 supplies the mezzanine circuits with power directly from the PSM. Connector P2 fans the protected supplies out to the XA1J2 and XA2J2 AFE connectors on the LCB. The circuits work individually to protect each AFE board and the PSM to allow a safe failure mode should an AFE board become inoperable. The following circuit descriptions will reference only the circuits that control and protect AFE1 since the AFE2 circuits are identical.

4.2 VANA Protection Circuit

Refer to schematic TRNT-EL-04-2003, page 1.

The VANA+ and VANA- supplies from the PSM enter the mezzanine board via pins 3 and 4 and pins 15 and 16 respectively of connector P1. The range of adjustment for these supplies allows them to have a valid input range of between +5V to +12V for the VANA+ and –5V to –12V for the VANA- supply. Each supply is referenced to the common ground potential on pins 2, 5, 6, 9, 1 and 17 of connector P1. This ground plane is connected directly to the 'single point ground' of the PSM. A hot swap controller IC from Linear Technologies (U34) controls both the negative and positive sides of this supply. The power supply for U34 is generated from the same supplies and applied to pins 1 and 16 of U34. These circuits provide current limiting and under voltage protection on the VANA supplies but do not provide overvoltage protection.

The signal **AFE1_PWR_EN_VANA** from pin 20 of P1 (and **AFE2_PWR_EN_VANA** for AFE2, pin 19 on P1) is used to control the supplies to the AFE boards. A voltage of >1.22V on pin 12 of U34 enables the hot swap controller. This signal comes from a 3.3V buffer on the LCB. The enable signal for the negative side on pin 6 is held enabled whenever the VANA- voltage is more negative than –4.85V. U34 holds the negative and positive side disabled until U34 pin 12 goes above 1.22 volts. When enabled, U34 begins to generate a positive potential on the **GATE+** signal (pin 14) and pull the **GATE-** signal (pin 4) more positive. These two gate signals drive the gate terminal of two N-Channel MOSFET devices (Q15, Q18) placed in series with the supplies to the AFE. The **GATE+** signal will drive to approximately 5 Volts above VANA+ to assure saturation of the gate on Q18. The **GATE-** signal on pin 4 will pull the gate of Q15 up to approximately 9 Volts above the VANA- potential to assure gate saturation for the negative series pass transistor. The turn on / off time is controlled by a combination of C7, R23, C8, R18, C5 and C6. The turn-on current is also limited by sensing the current through resistors R14 and R13 for the positive and negative supplies respectively. The initial

current is limited to 300ma and the limit rises linearly to limit the current at 1 amp when the supplies are fully enabled.

The fully enabled condition is identified when the **FB+** signal (U34 pin 13) and the **FB-** signal (U34 pin 5) are above / below 1.24 Volts. This is achieved when VANA+ supply is more positive than +5V and VANA- supply is more negative than –5V via the resistive dividers R136/R134 and R19/R21 and when Q18 and Q15 are fully turned on.

When stable operation is achieved the current through the MOSFET is continuously monitored via resistors R14 and R13. Should the potential across either of these resistors reach 50mv, the U34 device will time out a period of approximately 40ms before clamping the **GATE+** signal to ground and **GATE-** signal to VANA- thus shutting down and latching off the supply. To restart the supplies to the AFE, the ON+ signal is removed by setting **AFE1_PWR_EN_VANA** low and then raising this signal again to try a restart of the supply. Under fault conditions U34 pin 11 pulls low to provide a fault status signal to the LCB via the signal **/AFE1_PWR_FAIL_VANA**. This signal is an open collector input pulled high by a 4.7KOhm resistor to +3.3v on the LCB.

Amplifiers U32 and U33 provide a signal that is proportional to the actual current draw of the AFE on each supply. These devices accept common mode voltages at their inputs above their power supply potentials while amplifying the differential across the current sense resistors. The calibration value is set by resistors R12 and R124 to provide 1 Volt per Amp signal for telemetry purposes. These resistors are mounted directly on the LCB on later implementations of the system. The LCB telemetry circuits monitor the **AFE1/2_TI_VANA+** and **AFE1/2_TI_VANA-** output signals.

Reverse bias diodes D4 and D9 protect any circuitry on the AFE from reverse bias when one of the supplies has been shut down for any reason and leakage currents through the AFE cause the affected supply to be pulled toward the other. Diode arrays D3 and D7 protect the telemetry inputs to the LCB from any over voltage condition caused by a fault in the current telemetry amplifiers.

4.3 VCB Protection Circuit

Refer to schematic TRNT-EL-04-2003, page 2.

The VCB+ and VCB- supplies from the PSM enter the mezzanine board via pins 7 and 8, and pins 13 and 14 respectively of connector P1. The range of adjustment for these supplies allows them to have a valid input range of between +9V to +18V for the VCB+ and –9V to –18v for the VCB- supply. Each supply is referenced to the common ground potential on pins 2, 5, 6, 9, 1 and 17 of connector P1.

Two hot swap controller ICs from Texas Instruments (U26, U23) are used to control both the negative and positive sides of this supply. The power supply for U26 is taken directly from the VCB+ input. The power supply for U23 is generated by a constant current source from the VCB+ sourcing an internal shunt regulator in the UCC3913 device. When the VCB+ supply is on, U23 pin 3 is clamped to approximately 10 Volts above the VCB- supply voltage. These circuits provide current limiting and over / under voltage protection for the VCB+ and VCB- supplies.

U26 pin 1 is used to provide an undervoltage detection threshold for the VCB+ supply and a remote on/off controlled by an analog switch driven by the **AFE1_PWR_EN_VCB** signal. When this signal is set high from a buffer on the LCB, the analog enable switch (U19) opens allowing the voltage divider R41/R40 to sample the VCB+ supply potential. If the potential on pin U26 pin 1 is above its 1.38V threshold, this indicates that the VCB+ supply is above 9.95 Volts and the device can start to switch on the supply. If these input conditions have been met the device begins to ramp the **GATE** signal (U26 pin 8) high.

The **GATE** signal will ramp up to approximately 13 Volts above the VCB+ supply potential to properly bias the MOSFET Q16 used as a series pass element to the AFE board. The rate of rise on the **GATE** signal is controlled by R45, C16 and C15 to provide a slow voltage turn on. In addition, during this turn-on period the current drawn by the AFE is measured and the voltage drop across the Q16 is monitored to generate a constant power ramp of approximately 750 mw. The slope of this power ramp is controlled by the potential on U26 pin 3 (nominally 150mv) developed by the voltage divider resistors R43/R42. If the fault timer times out (U26 pin 4 reaching 4 Volts) during the startup phase, the **GATE** output of U26 is clamped to ground and the start up aborted. This may happen if an excessively large capacitor is placed as a bulk charge device on the AFE board supply input or if there is a short circuit present on the AFE hardware.

Once stable operation is obtained (VCB+ > 9.95V, VCB+ current less than 0.5 Amps) the circuit will monitor current via R32 and U26 pin 9 and power dissipation in the MOSFET device via U26 pin 7. Should the current increase to the limit of 0.5 Amps or Q16 dissipation be above 750mw, the timer pin begins to charge C14 via a 25μa source. When this pin reaches 4.0 Volts the device goes into overcurrent shutdown mode by clamping the **GATE** output to ground. To recover the operation of the supply the **AFE1_PWR_EN_VCB** signal must be taken low and then high again to initiate another start cycle. During a fault condition or when the supply is not enabled, U26 pin 6 (PG) is pulled low. This signal has a wire or connection to the VCB- supply protection device. It is labeled **/AFE1_PWR_FAIL_VCB** on the schematic and is pulled high by a 4.7KOhm resistor to +3.3V on the LCB.

If the VCB+ supply potential exceeds 20 Volts, the Zener diode (D34) begins to conduct and force the timer input (U26 pin 4) to a potential above ground. When approximately 24 Volts is reached on the VCB+ supply, the timer input on U26 pin 4 will be forced to 4.0 Volts and U26 will shut down the supply to the AFE board.

Supply protection for the VCB- supply is provided by U23. U27, an analog switch, is used to hold the signal **SD/FAULT** (U23 pin 1) at a potential above 2.0 Volts by forcing a nominal 100μa source from the shunted power supply potential of U28 into the shutdown pin. When U23 pin 6 is taken above the logic threshold voltage of approximately 2.4 Volts above ground, the 100μa current source is removed and the device begins to turn on. During turn-on the potential on U23 pin 7 begins to rise towards VDD on pin 3 of U23 thus turning on the series pass MOSFET transistor Q12. The ramp timing for this transition is controlled by C30, C18 and R56. In addition, the device uses active current limiting to avoid inrush current excursions above the nominal current limit of 0.5 Amp.

When under normal conditions, that is VCB- current < 0.5 Amps, the gate voltage on Q12 should be approximately 10 Volts above the VCB- potential. If the VCB- supply becomes more negative than 20 Volts the Zener diode D12 begins to conduct. When the supply exceeds approximately 22.5 Volts the potential on U23 pin 4 will cause the hot swap device to go into shutdown mode. This device will latch the supply off to the AFE while the potential on VCB- exceeds the threshold. The hot swap controller will also enter shutdown mode if the current through R54 exceeds 0.5 Amps for more than 55 ms. However, under these conditions the fault will not be latched and the hot swap controller will attempt to restart after approximately 20 seconds.

Under any fault condition the hot swap device will drive pin 1 high to approximately 8 Volts, which is connected to the gate of transistor Q11. Q11 has its source connected to the VCB- supply and the drain connected to a voltage divider formed by the R117 and the 4.7KOhm resistor to +3.3V pull-up on the LCB. This signal is in common to the fault condition flag of the VCB+ supply. The resistive

divider provides a safe range to allow the buffer on the LCB to detect a fault condition on either supply.

The current monitor amplifiers U25 and U20 provide the LCB with a telemetry voltage proportional to the current consumption of the AFE for the supplies.

The calibration values are set by resistors R31 and R53 to provide a 2 Volts per Amp signal for telemetry purposes. These resistors are mounted directly on the LCB on later implementations of the system. The LCB telemetry circuits monitor the **AFE1/2_TI_VCB+** and **AFE1/2_TI_VCB-** output signals.

Reverse bias diodes D35 and D19 protect any circuitry on the AFE from reverse bias when one of the supplies has been shut down for any reason and leakage currents through the AFE cause the affected supply to be pulled toward the other. Diode arrays D33 and D16 protect the telemetry inputs to the LCB from any over voltage condition caused by a fault in the current telemetry amplifiers.

4.4 VHV Protection Circuit.

Refer to schematic TRNT-EL-04-2003, page 2.

The VHV+ and VHV- supplies from the PSM enter the mezzanine board via pins10 and 12 respectively of connector P1. These supplies provide high voltage bias for CCD detectors and have an input range of either +30 Volts (VHV+) –5 Volts (VHV-) for N-Channel detectors or +5V (VHV+) and –30V (VHV-) for P-Channel detectors. The selection of the mode, N or P channel, of the supplies is done in the PSM via a relay controlled by the signal **VHV_POL_SLCT**. The supplies are referenced to the common ground potential on pins 2, 5, 6, 9, 1 and 17 of connector P1.

The circuit topology is similar to those described for the VCB supplies. A Linear Technology (LT4356) surge controller device (U3) is used to control and protect the VHV+ supply. This device is powered from the same supply and enabled when U3 pin 9 is left floating by U9, the analog switch, commuting in response to the signal **AFE1_PWR_EN_VHV** sourced by the LCB going high to +3.3V. When enabled, the **GATE** pin (U3 pin 4) begins to rise and turns on transistor Q7 after exceeding the gate threshold voltage of approximately 4 Volts. If the startup conditions are correct, the gate voltage will settle at a potential of approximately 8V above the VHV+ supply value to assure saturation of the series pass transistor.

The LT4356 has an uncommitted amplifier that is used to detect in which mode the supply is operating. R74/R75 form a voltage divider that supplies U3 pin 16 with a voltage above 1.25V when the supply is at +30V for N-Channel mode and below 1.25V when the supply is at +5V potential for P-Channel mode. The output of this amplifier appears on U3 pin 14 and is connected to the base of Q3. When the supply operates in N-Channel mode this transistor is biased on and shunts the feedback divider formed by R66/R72 with another resistor R71 to correctly supply the feedback pin (pin 2) of the LT4356 with the output status. This signal detects any overvoltage condition on this supply.

If the feedback pin (U3 pin 2) exceeds 1.25V (which corresponds to 34 Volts in N-Channel mode or 7v in P-Channel mode) U3 begins to charge C27 through U3 pin 1. When U3 pin 1 reaches 1.25V (approximately 30ms after a fault condition) the device will pull down the fault indicator on pin 10. This signal has a wire or connection to the VHV- and the AFE2 fault indicators. It produces a signal called AFE_PWR_FAIL_VHV that is used as status information by the LCB. The voltage on U3 pin 1 continues to rise until a value of 1.35V is reached at which point the gate signal is clamped to ground and the supply is shut down to the AFE. During this time the supply to the AFE is maintained and clamped to a potential corresponding to a value of 1.25V at the feedback pin (34V or 7V depending on the mode).

The overvoltage protection circuit on this device allows an automatic restart after the supply shutdown that occurs after approximately 1 second. Under conditions of over voltage in N-Channel mode an additional protection circuit formed by D17 and R67 is employed to lock off the circuit. At approximately 33V the Zener diode (D17) supplies charge current to capacitor C27 and maintains U3 pin 1 at above 1.35V which effectively disables the device from turning on.

An over current protection scheme is active with this device when the potential across R57 exceeds 50mv or the potential between the Q7 drain and Q7 source terminals exceeds 0.5V. Under either of these conditions the timer circuit is enabled and after a delay proportional to the extent of the fault, the fault signal is asserted and supply shutdown occurs.

The negative power supply protection circuit employs a hot swap controller device (U5) from Texas Instruments (UCC3913). Circuit topology is very similar to the VCB- supply protection circuit. U5 is supplied from a constant current source (U1) to provide 4ma of current for the internal regulator to develop 10 Volts on U5 pin 3 above the VHV- supply potential. This supply is also used to switch in a 100µa current source via analog switch U10 to hold the **SD/FLT** signal at a high potential and disable the supply output to the AFE. When the analog switch commutes on command by the **AFE_PWR_EN_VHV** signal this pin is pulled low internally by U5 and the startup process for enabling the VHV- supply begins.

During turn-on the potential on U5 pin 7 begins to rise towards VDD (U5 pin 3) thus turning on the series pass MOSFET transistor Q5. The ramp timing for this transition is controlled by C22, C23 and R84. In addition, the device uses active current limiting to avoid inrush current excursions above the nominal current limit of 0.2 Amp.

When under normal conditions, that is VHV- current less than 0.2 Amps, the gate voltage on Q5 should be approximately 10 Volts above the VHV- potential. Note that this potential relative to ground depends on the mode that the supply is operating in. The potentials for the control device (U5) are all referenced to the VSS node at U5 pin 5. If the VHV- supply becomes more negative than 31 Volts the Zener diode D22 begins to conduct. When the supply exceeds approximately 32.5 Volts the potential on U5 pin 4 will cause the hot swap device to go into shut down mode. This device will latch the supply off to the AFE while the potential on VHV- exceeds the threshold. The hot swap controller will also enter shutdown mode if the current through R70 exceeds 0.2 Amps for more than 55 ms. However, under these conditions the fault will not be latched and the hot swap controller will attempt to restart after approximately 20 seconds.

Under any fault condition the hot swap device will drive pin 1 high to approximately 8 Volts above VSS. This pin is connected to the gate of transistor Q1. Q1 has its source is connected to the VHV- supply and the drain connected to a voltage divider formed by the R60 and the 4.7K-Ohm resistor to +3.3V pull-up on the LCB. This signal is in common to the fault condition flag of the VHV+ supply and is common to both AFE1 and AFE2 circuitry. The resistive divider provides a safe range to allow the buffer on the LCB to detect a fault condition on either supply.

The Current monitor amplifiers U12 and U4 provide the LCB with a telemetry voltage proportional to the current consumption of the AFE for the supplies.

The calibration values are set by resistors R58 and R82 to provide a 5 Volts per Amp signal for telemetry purposes. These resistors are mounted directly on the LCB on later implementations of the system. The LCB telemetry circuits monitor the **AFE1/2_TI_VHV+** and **AFE1/2_TI_VHV-** output signals.

Reverse bias protection diodes D28 and D24 protect any circuitry on the AFE from reverse bias when one of the supplies has been shut down for any reason and leakage currents through the AFE cause the

affected supply to be pulled toward the other. Diode arrays D14 and D26 protect the telemetry inputs to the LCB from any over voltage condition caused by a fault in the current telemetry amplifiers.

4.5 VBB_Det Route-through

Refer to schematic TRNT-EL-04-2003, page 1.

The mezzanine board carries a single trace connected directly between connector P1 pin 1 and connector P2 pin 4. This trace is currently reserved to provide connectivity between the LCB and the AFE boards for a high voltage backside bias telemetry signal. This trace is specified for 80v at a current of up to 200μa. The signal name for this trace is **DET_VBB_TV**. It is not currently used.

5.0 CCD Analog Front End Board (CCD AFE)

Refer to schematic TRNT-EL-04-2004.

This description corresponds to Revision –C1– of the hardware.

The Analog Front End board is responsible for the generation of detector specific clock and bias signals and the acquisition and analog to digital conversion of up to four channels of detector video signal. There is provision to fit two identical AFE boards to the LCB. The AFE boards must locked to the LCB using the AFE board latch mechanism to secure the board to the LCB connector. Failure to use the mechanical board latch will result in unpredictable behavour of the AFE board.

Most of the circuitry on the AFE board is directly controlled by the values written to attribute registers in the LCB FPGA. The action of writing a value to an attribute in the LCB triggers the process to transfer the value to the appropriate hardware of the AFE.

5.1 Interface Circuits.

Refer to schematic TRNT-EL-04-2004, page 1.

The selection and addressing between these two boards by the LCB is generated by the FPGA and accomplished using two distinct methods.

In the first method: The odd / even pin designations are swapped for the two AFE connectors XA1J2 and XA2J2 on the LCB for the signal groups PWRDATA(73:72), PWRDATA(71:68), PWRDATA (67:64), PWRDATA(63:60), PWRDATA(59:44), PWRDATA(35:0), CLKBIAS(91:88), CLKBIAS(87:84), CLKBIAS(83:82), and CLKBIAS(81:80). The PWRDATA signal groupings provide the AFE with dedicated alternate signal busses without having to multiplexing their outputs i.e. even pins are dedicated to AFE1 data paths, odd pins are dedicated to AFE2 data paths. This provides for the principle method of acquiring data from the AFE. The CLKBIAS signal groups provide the LCB with odd / even strobes to select the appropriate AFE to deliver control data to the AFE board using common signal busses.

In the second method: The LCB signals are bussed to each AFE connector using the same connector pin designations and separate strobes (as described above) are used to latch data to the AFE interface. Signal groups using this method are PWRDATA(43:36), CLKBIAS(79:0).

The interface signals entering the AFE are driven from the LCB using voltage translation devices that permit using an intermediate voltage for driving the AFE interface receiver latches. This voltage is controlled by the VPIFC (Voltage Positive Interface) supply and is sourced from the local AFE 3.3 volt logic power supply when the AFE has VANA+ power applied to it i.e. the AFE is powered up and enabled. This supply is used for all AFE interface control input latches and strobe receivers (U63, U107, U55, U149, U146, U41, U141, U110[(1)]). When the AFE is powered off the VPIFC supply is derived from the LCB 3.3v logic supply via pin 1 and 2 of the AFE clock and bias connector P1.

[(1)] U110 is currently powered from the AFE 3.3v supply – it should be powered from the VPIFC supply !

The control input latches are enabled using remotely from the LCB interface by asserting the AFE_CTRL_ENABLE signal. Q1 and Q2 (page 3) act as a half bridge circuit to strongly pull the latch enable signals to their respective logic states. This is required since when the AFE is not powered up the current leakage through the latch inputs to the un-powered output signal devices and hence through to the AFE power supply rail causes an indeterminable state on the DAC devices.

The interface control input latches use strobes to latch the control data for their specific purpose. These strobes are produced by the LCB FPGA and passed through the AFE Gateway firmware logic to produce the correct setup time for the data to the latches.

Device U63 pin 6 provides the strobe to latch CDS state data to U117 and U102 dependent on the latch enable signals AFE_CHANSLCT(3:0). These enable signals are generated by the LCB FPGA from the bit mask **CdsChanSlctReg** attribute value. The CDS state that is latched into U117 and U102 is controlled by the value of the **CdsStateReg** attribute value. The state information written to CDS channel 4 can be sampled at test connector JT1. Table 16 shows the state significance of the attribute value:

Table 16 - CDS State functions from CdsStateReg attribute value

Bit	CDS state signal	Function
0	CNVTST	Command to Convert (CTC) – Triggers an ADC conversion cycle
1	INV	Presents an inverted video signal to the integrator stage
2	NONINV	Presents a non-inverted video signal to the integrator stage
3	INTEGRATE	Enables the integration stage to integrate
4	DCRESTORE	Clamps the AC input stage of the signal processor to restore the zero point
5	RESET	Resets the integrator stage
6		Not used
7		Not used

Device U63 pin 4 provides the strobe to latch clock state information to U149 to control the clock state switches. The value of the data written to the latch is controlled by the **AfeClkStateReg** attribute value.

Device U55 pin 6 produces a strobe to write data to the control input latches U146, U41 and U141. Data written to U146 controls the test point circuitry and the clock bank enables for the AFE. The TP_RST signal is not used in the current firmware.

Data written to latch U41 controls the loading of serial data to the DAC and Telemetry circuits. The DAC_SDIN conveys a serial data stream used to load data values to the DAC and telemetry multiplexor devices. The TELADC_DIN is a serial data stream used to control the telemetry ADC devices. The SYNC signals are used to address a particular device connected to the serial data streams to load data to the selected device. The DAC_LDACn signals are not used in the current firmware.

Latch device U141 carries the bias bank enable signals and the serial data stream synchronization clocks. The DAC_SCLK and TEL_SCLK signals are synchronous to the serial data streams and respective SYNC signals produced from latch U41. The telemetry serial data interface is run slower than the dac serial data interface. DAC_SCLK runs at approx. 20 MHz and TEL_SCLK at approx. 5MHz for data transfers. The DAC_PDn (Power Down) and DAC_CLRn signals are not used in the current firmware release. The DAC_RESET signal is used only when the AFE board is powered on.

The test points (TP46, 50, 47, 52, 63-66) can be used to effectively confirm correct serial data interface signals. The format of the serial data is different for each device attached to the serial busses (see this document).

Data passing through the interface from the AFE to the LCB is latched and timed by U100. There are two types of data that are passed to the LCB. Pixel data from the video signal processor ADC devices, telemetry data, and the DAC readback data are serial data streams synchronized to their respective data clocks (AFE_ADC_STB, DAC_SCLK and TEL_SCLK respectively). This data is latched into U100 by the strobe AFE_DATA_STB generated by the LCB FPGA. The DAC_BUSYn signals are logic level status indicators used to synchronize the communications to the AFE Gateway firmware logic. These last group of signals are sampled whenever a DAC device is being updated with a new value.

5.2 Local Power Supplies.

Refer to schematic TRNT-EL-04-2004, page 3.

The AFE design requires ten separate power supplies to fulfill its function. All of these supplies are derived from six 'Analog' power rails supplied to the AFE board via the LCB-MEZ hardware. The incoming and derived power supplies are detailed in Table 17.

Table 17 - AFE Power supplies

Input Supply	Min (Volts)	Max (Volts)	Max input (ma)	Internal Supply	Test Point	Purpose
VANA+	+5.0	+11.5	360	+3.3v	TP3	Digital logic -CDS latch, DACs, TP latches
				+5va	TP45	Reference buffers, telemetry ADCs, telemetry muxes, telemetry amplifiers, clock state switches, Bias and clock DAC reference
				+5.5v	TP35	Video offset DAC reference, video ADC offset reference, video ADC power, video amplifiers
				+10v	TP71	Video switches, video ADC reference, preamp power.
VANA-	-5.0	-11.5	360	-5v	TP31	Video amplifiers
				-10v	TP72	Video switches, preamp power.
VCB+	+9.0	+18.0	325	+VALO	TP59	Clock and bias amplifiers, clock and bias isolation switches, clock and bias test point switches.
VCB-	-9.0	-18.0	325	-VALO	TP62	Clock and bias amplifiers, clock and bias isolation switches, clock and bias test point switches.
VHV+	+5.0	+30.0	100	+VAHI	TP48	High voltage bias amplifiers and isolation switches, High voltage test point switches.
VHV-	-5.0	-30.0	100	-VALO	TP53	High voltage bias amplifiers and isolation switches, High voltage test point switches

The High Voltage supply for the AFE has an auto-commute function that detects the magnitude of the voltage present on the HV+ supply input to adjust the regulator output setpoints. This is achieved via resistive divider R49/R82 and analog switch U153. When the switch control input (U153 pin 3) reaches the threshold voltage of the control input the switch opens so that the set point voltage for

U56 is set to 31.6 volts by resistor R73. This threshold is reached when the VHV+ power supply is approximately 20 volts. When the HV+ supply is below 16 volts the switch de-activates and forces the set point for U56 to be controlled by R73 in parallel with R72. This sets the output voltage for U56 to be 2.3 volts. The negative high voltage regulator represented by U67 simply derives an output voltage that is 31 volts below the +VAHI value through resistors R87 and R255.

Reference voltages used by the AFE bias and clock circuitry are derived from the outputs of U21 and U62. These references are buffered to provide current to these circuits. U123 supplies the reference voltage for the video processor offset DAC and offset amplifier reference circuits.

The VPIFC supply is derived through a reverse bias blocking diode (D1) to provide the interface latch power supply. This supply overrides the VPIFC supplied by the LCB board when the AFE board is powered down.

5.3 DAC Interface Circuits.

Refer to schematic TRNT-EL-04-2004, page 1.

There are four DAC devices used in the AFE design with 12-bit resolution. These DACs provide the reference for the high state and low state clock voltages, the bias and high voltage bias voltages, and the video processor channel offset voltages. The DACs (U13, U27, U48, and U92) are all controlled by the common serial data interface comprising of DAC_SCLK, DAC_SDIN, DAC_SDOUTn, DAC_BUSYn, and DAC_SYNCn signals. The device load and clear pins (pins 39 and 1) are not used in the current firmware control scheme. Each DAC has sixteen channels that provide a buffered output between 0 and 5 volts referenced to ground when using an external reference of 2.5 volts on pin 5. These outputs are then amplified by their associated amplifiers to provide the voltages that are used to condition a detector during operation.

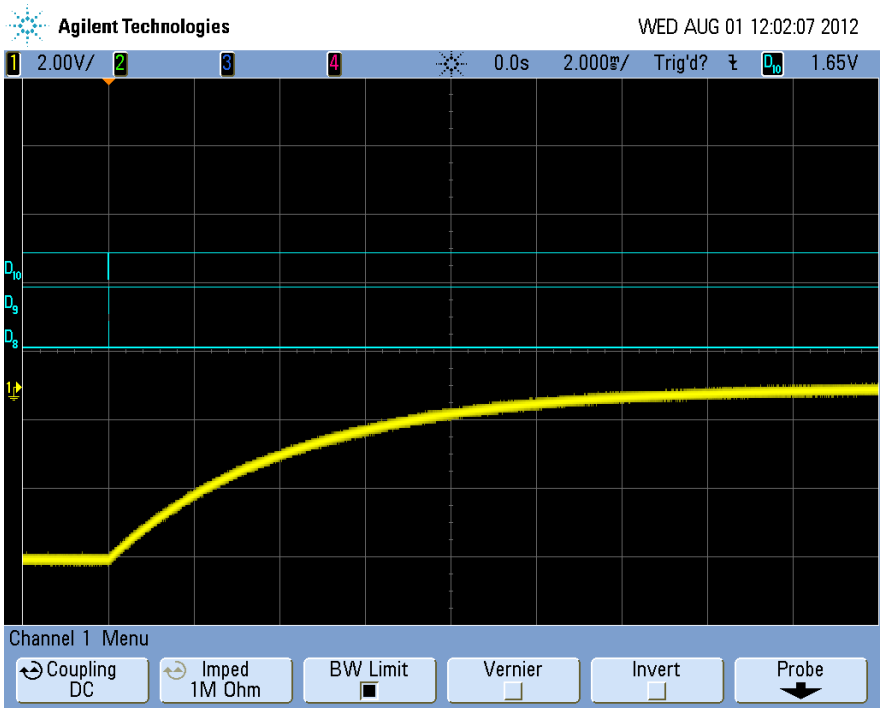
The DACs are unipolar devices but the dynamic range of their operation is converted to bipolar mode by offsetting the feedback node of the amplifiers attached to the outputs of the DAC. In this way each DAC controls a voltage range that is settable to a positive or negative value.

When it is necessary to update the value of a DAC output (by writing a new value to a DAC setting attribute in the LCB) the LCB FPGA generates a clock waveform on the DAC_SCLK. Synchronous to this clock, the FPGA generates the appropriate low true /DAC_SYNCn signal to enable the device for receiving the serial data stream on DAC_DIN. A valid write frame is 24-bits of data that are written to the DAC and the frame is terminated by taking the /DAC_SYNCn signal false (high). The DAC acknowledges the success of the write cycle by taking the appropriate /DAC_BUSYn signal low. The /DAC_BUSYn signal remains low until the DAC has updated its internal register and the voltage of the selected channel output is slewing to the new value. Since the low-true /DAC_LDACn signals of the DAC are held low, the output channel updates immediately after the successful write transaction.

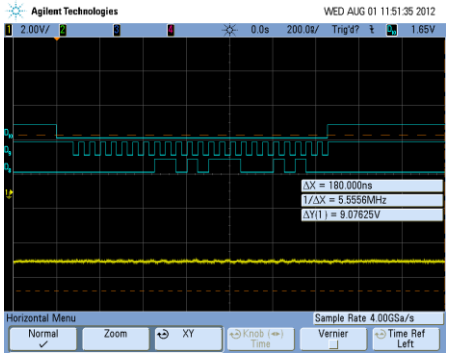
The DAC devices allow for a monitoring channel (MONOUT) that outputs the value of the DAC output channel driver divided by 2. This feature is used with firmware to allow diagnostics to be performed on the AFE board. When using this feature the appropriate DAC must be scanned by setting the **TelScanCmd** attribute to a suitable value (when the periodic scanning is turned off) and viewing the results in the **Afe1(2)AuxTelReg(15:0)** attributes.

Figure xx shows a typical DAC load transaction. The AFE2 bias0 signal was originally set to -5.0 volts and was then set to 0 volts. Note that the bias output settling time is approx. 20ms. The DAC write transaction takes approx. 1.25us to complete.

Figure 6 – DAC Write timing



Trace	Signal
D8	DAC_SDIN (TP47)
D9	DAC_SCLK (TP46)
D10	/DAC_SYNC0 (TP63)
Yellow	AFE2 bias 0 output (J1:13)



5.4 Clock Driver Circuits.

Refer to schematic TRNT-EL-04-2004, pages 4 and 5.

There are sixteen identical clock channels available on each AFE board. These clock signals normally provide the detector conditioning required to read out a charge coupled detector. The voltage of the high and low rails are adjustable between limits of +/-VCB (nominally +/-18v). This description uses the references associated with clock channel 0 to illustrate the operation. Each clock has an associated state switch (U28), amplifier (U32A), telemetry pick-off (R378/R379), and isolation switch (U8) associated with it. The outputs of the clock high and low voltage DACs are present on U28 pins 6 and 4. These would have been set to the desired voltages prior to enabling the clock group and connecting a detector to the clock channel. The state of U28 is controlled via signal CLKSTATE0 from the control input latch U149 which reflects the value of the **AfeClkStateReg** attribute.

The selected voltage is divided by resistors R21/R22 with a ratio of 0.877 to provide voltage to drive to the non-inverting node of U32A. The voltage on the non-inverting node of U32A is amplified by a factor of 8.14 to produce the clock voltage for the detector. The gain resistor reference for U32A is forced to a value of +2.5v and the inverting gain of the amplifier is -7.14 so when the non-inverting node is at a voltage of 0 volts i.e. DAC output at zero volts, the output will slew to a value of -17.85 (2.5 x -7.14).

When the DAC is set to a value that represents half the dynamic range of the DAC (i.e. 2047), the voltage present at the switch will be close to +2.5v. This voltage is reduced by the resistive dividers to

produce +2.2175 volts and amplified by the non-inverting gain of U32A (8.14) to produce an output from U32A of approx. (2.2175 x 8.14 + -17.85) volts i.e. approx. 200mv.

When the DAC is set to the full-scale value (i.e. 4097), the voltage at the non-inverting node of U32A will be approx. +4.385 volts. The output of U32A will now settle at (4.385 x 8.14 + -17.85) volts i.e. approx. +17.84 volts.

Current feedback amplifiers are used for the clock drivers to provide a fast slew rate when used with capacitive loads. The slew rate at the amplifier for 90% of the dynamic range should be less than 90ns. C445 in the feedback loop of the amplifier can be used to roll off the high frequency response of the amplifier to critically damp the output under different operating conditions. Resistor R370 is used to buffer capacitive loading of the detector and wiring harness from the amplifier output stage and promote stability.

Resistors R378/R379 are used to pick-off and condition the clock voltage to supply a signal for telemetry. The divider has a ratio of 0.1226 and is sourced on one end of R379 by a +2.5v reference to shift the bipolar clock signal range into a unipolar range of 0.3 ⇔ 4.7v. The telemetry pick-off is fed to a multiplexor that selects the individual clock voltages for conversion by a 12-bit ADC which provides for an approx. 10mv resolution.

The outputs of the clock amplifiers are fed to the isolation switch U8. This device isolates the active clock signals from the detector while they are uninitialized or while shutting the system down. The switch is activated and the clock outputs enabled when the control signal on U8 pin 1 is high. The control signals for U8 and the other clock banks switches (U9, U10, U12) are directly linked to the **ClkEnbl** attribute value. These signals are also conditioned by U147 that represents the state of the LCB watchdog timer. This enables an immediate isolation of the clock signals from the detector in the event that the LCB looses its primary clock source when the DHE is functioning as a slave in a multi-DHE application.

5.5 Low Voltage Bias Circuits.

Refer to schematic TRNT-EL-04-2004, page 6.

The low voltage bias circuits have a very similar topology to the clock driver circuits described previously in section 5.4. There are eight identical low voltage channels available on each AFE board. These bias signals normally provide the low noise dc potentials for such things as last gate and substrate bumping that a charge coupled detector uses to move charge through its registers. The voltages of each low voltage bias is adjustable between limits of +/-VCB (nominally +/-18v). This description uses the references associated with bias channel 0 to illustrate the operation.

Each bias has an associated low pass filter (R301/C52), a voltage divider (R301/R310), an amplifier (U51A), a telemetry pick-off (R58/R308), and an isolation switch (U54) associated with it. The channel 0 output of the bias voltage DAC (U48) is divided and filtered by the R301, C52, and R310 network to provide a low noise potential to the non-inverting node of U51A. The ratio of the divider is 0.878 with a low pass 3db cutoff frequency 32 Hz. This voltage is amplified by U51A with a gain of +8.21. The inverting node has a gain of 7.21 and one end of the gain resistor is held at +2.5v. When the bias DAC channel 0 output is at 0v the output of the bias amplifier will be at approx. -18.0 volts (0 x 8.21 + 2.5 x -7.21).

When the DAC is set to a value that represents half the dynamic range of the DAC (i.e. 2047), the voltage present at the DAC output will be close to +2.5v. This voltage is reduced by the resistive dividers to produce +2.2195 volts and amplified by the non-inverting gain of U51A (8.21) to produce an output from U51A of approx. (2.2195 x 8.21 + 2.5 x -7.21) volts i.e. approx. 200mv.

When the DAC is set to the full-scale value (i.e. 4097), the voltage at the non-inverting node of U51A will be approx. +4.39 volts. The output of U51A will now settle at (4.39 x 8.21 + 2.5 x -7.21) volts i.e. approx. +18.0 volts.

Bipolar voltage feedback amplifiers are used for the bias drivers to provide low noise and an output current capability of 20ma. The slew rate at the amplifier is limited by C388 in the feedback loop of the amplifier to roll off the high frequency response of the amplifier and enhance stability. There are no resistors in the output to enable the full power of the amplifier. Further filtering and/or current limiting can be done by using options in the TSM-PRE module.

Resistors R58/R308 are used to pick-off and condition the bias voltage to supply a signal for telemetry. The divider has a ratio of 0.1226 and is sourced on one end of R308 by a +2.5v reference to shift the bipolar clock signal range into a unipolar range of 0.3 ⇔ 4.7v. The telemetry pick-off is fed to a multiplexor that selects the individual bias voltages for conversion by a 12-bit ADC which provides for an approx. 10mv resolution.

The outputs of the low voltage bias amplifiers are fed to the isolation switch U54. This device isolates the active bias signals from the detector while they are uninitialized or while shutting the system down. The switch is activated and the bias outputs enabled when the control signal on U54 pin 1 is high. The control signals for U54 and the other low bias bank switches U47 are directly linked to bits 0 and 1 of the **BiasEnbl** attribute value (for AFE1. For AFE2 the lv-bias enable bits are 4 and 5). These signals are also conditioned by U142 that represents the state of the LCB watchdog timer. This enables an immediate isolation of the low voltage bias signals from the detector in the event that the LCB looses its primary clock source when the DHE is functioning as a slave in a multi-DHE application.

5.6 High Voltage Bias Circuits.

Refer to schematic TRNT-EL-04-2004, page 7.

The high voltage bias circuits have a very similar topology to the low voltage bias circuits described previously in section 5.5. There are eight identical high voltage channels available on each AFE board. These bias signals normally provide the low noise dc potentials for such things as detector output amplifier and reset transistor drain potentials. The voltages of each high voltage bias is adjustable between the limits of the VHV power supply capability (i.e. nominally +/-30v). The polarity of these bias voltages is controlled by the **VhvPolaritySlct** attribute. This description uses the references associated with bias channel 0 to illustrate the operation and assumes that the polarity is selected for the appropriate mode i.e. positive or negative potentials.

Each bias has an associated low pass filter (R289/C62), a voltage divider (R289/R279), an amplifier (U49B), a telemetry pick-off (R64/R276), and an isolation switch (U53) associated with it. The channel 8 output of the bias voltage DAC (U48) is divided and filtered by the R289, C62, and R279

network to provide a low noise potential to the non-inverting node of U49B. The ratio of the divider is 0.918 with a low pass 3db cutoff frequency at 32 Hz. This voltage is amplified by U49B with a gain of +12.26. The inverting node has a gain of 11.26 and one end of the gain resistor (R56) is held at +2.5v. When the bias DAC channel 0 output is at 0v the output of the bias amplifier will be at approx. (0 x 12.26 + 2.5 x -11.26) i.e. -28.2v.

When the DAC is set to a value that represents half the dynamic range of the DAC (i.e. 2047), the voltage present at the DAC output will be close to +2.5v. This voltage is reduced by the resistive dividers to produce +2.295 volts and amplified by the non-inverting gain of U49B (12.26) to produce an output from U49B of approx. (2.295 x 12.26 + 2.5 x -11.26) volts i.e. approx. 13mv.

When the DAC is set to the full-scale value (i.e. 4097), the voltage at the non-inverting node of U49B will be approx. +4.59 volts. The output of U49B will now settle at (4.59 x 12.26 + 2.5 x -11.26) volts i.e. approx. +28.12 volts.

If the DAC output is programmed for a voltage output that does not correspond to the polarity mode in use the output of the amplifier will saturate and clamp at a value close to either the lower or upper power supply rail depending on the polarity mode. When this occurs, a small (but potentially dangerous) DC level will be present on the high voltage bias channel. The magnitude of this voltage is of order 2.5 volts. Be careful during operation to first establish the polarity that is required for the detector and then limit – by software – any attempt to set a high voltage bias to the opposite polarity. The TSM-PRE module has provision for fitting protection diodes to the high voltage bias channels as a fail safe measure against this possibility.

The amplifier used in this circuit is a hybrid Bipolar / FET input, voltage feedback amplifier which provides high stability and capabilities for driving large capacitive loads. This amplifier is low noise and with an output current capability of 30ma. The high frequency response of the amplifier is limited to approx. 6 Hz by C385 in the feedback to enhance stability. There are no resistors in the output to enable the full power of the amplifier. Further filtering and/or current limiting can be done by using options in the TSM-PRE module.

Resistors R54/R304 are used to pick-off and condition the bias voltage to supply a signal for telemetry. The divider has a ratio of 0.0814 and is sourced on one end of R304 by a +2.5v reference to shift the bipolar clock signal range into a unipolar range of 0.2 ⇔ 4.8v. The telemetry pick-off is fed to a multiplexor that selects the individual bias voltages for conversion by a 12-bit ADC which provides for an approx. 14mv resolution.

The outputs of the high voltage bias amplifiers are fed to the isolation switch U53. This device isolates the active bias signals from the detector while they are uninitialized or while shutting the system down. The switch is activated and the bias outputs enabled when the control signal on U53 pin 1 is high. The control signals for U53 and the other high voltage bias bank switch U46 are directly linked to bits 2 and 3 of the **BiasEnbl** attribute value (for AFE1. For AFE2 the hv-bias enable bits are 7 and 8). These signals are also conditioned by U142 that represents the state of the LCB watchdog timer. This enables an immediate isolation of the high voltage bias signals from the detector in the event that the LCB looses its primary clock source when the DHE is functioning as a slave in a multi-DHE application.

5.7 Video Signal Processing Circuits.

Refer to schematic TRNT-EL-04-2004, pages 8 and 9.

There are four separate and identical video channels on each AFE board. This description will use the AFE channel 1 video circuit as a reference to the other three channels. These circuits are designed to process the video signal output from a charge coupled detector using the classical correlated double sample (CDS) method.

The detector video signal is first amplified by the circuitry on the TSM-PRE module and sent from the TSM via the video flex circuit interface to provide an input to the video processor circuit on the AFE.

Input buffer and clamp circuit

The input signal from the preamplifier is sampled by amplifier U83 to provide a 'raw' video diagnostic signal available on the AFE test point TP34 which can be used as a reference when setting up and/or diagnosing problems with the circuit.

The input signal from the TSM-PRE is filtered by the combination of R235 and C309 to roll off the high frequency response of the circuit above 8 MHz to reduce the white noise contribution from the detector amplifier and TSM preamplifier sources. The input impedance characteristic of the AFE video channel is complex due to the clamping function of U79 so the preamplifier needs to be able to source the changing current requirements (i.e. low impedance) whilst not be disturbed by the abrupt impedance changes (i.e. stable) and still be able to settle in a finite time for the pixel to maintain precision (i.e. fast).

Capacitor C104 acts as a the AC coupling device to the buffer amplifier U80. This amplifier, a FET input type with a high impedance input, is set at unity gain is used to reduce the source impedance of the video signal after the AC coupling stage.

The video input signal at the input to U80 is periodically clamped on each pixel cycle by the analog switch U79. This switch discharges any DC offset from charge pumping on C104 due to the high impedance input and bias currents from U80 itself. This ensures that each pixel is processed using the same DC baseline in the video processing stages to follow.

Signal polarity inversion

After the impedance conversion of U80, the video signal is fed the signal polarity stage comprising of U77 and U130. This circuit uses the analog switch U77 to commutate the input signal between inverted or non-inverted output of U130 to supply to the signal integrator stage. The non-inverting mode is selected (under control of the LCB FPGA). By setting U77 pins 1 and 16 at digital high (true) levels and pins 9 and 8 at digital low (false) levels. In this configuration switches 1 and 2 of U77 are conducting. This configuration is normally used when the CDS integrator is sampling an N-Channel detector pixel charge signal level. In this configuration the input signal is divided by R249A and R249B to half its original magnitude and sourced through U77 switch 1 to the non-inverting node of U130. The feedback circuit from the output of U130 is divide by two by the resistive divider formed by R242A and R242B and then fed through switch 2 to the inverting node of U130. The non-inverting gain of U130 is 2.0 while the input signal present on the non-inverting node is half the original signal so the net gain is 1.0 i.e. you should see the same signal on TP42 as you do on TP40.

In the inverting mode, usually used when sampling the detector reset potential in an n-channel detector, U77 pins 9 and 8 are high and U77 pins 1 and 16 low. U77 switches 3 and 4 are conducting and the input signal is fed via R245A and through U77 switch 3 to the inverting node of U130. The feedback path is from the output of U130 via R245B to form the virtual ground point. The non-inverting node of the U130 is clamped to ground potential via U77 switch 4 and R92. In this configuration R242A and R242B act as a 1K Ohm load on the output of the amplifier. In this configuration the gain of the circuit is controlled by the ratio of R245A to R245B and is -1 i.e. on TP42 you see an inverted copy of the signal on TP40.

It is possible (and advisable) to inject the input signal as a common mode source to the amplifier when large input signal levels might be encountered and during the transition between non-inverting and inverting modes. By setting all U77 switches on, the amplifier 'sees' the input signal on both input nodes and remains at the zero point of operation. It is not advisable to operate this circuit in open mode i.e. with all U77 switches off. In this condition the amplifier has no input signal, input reference or feedback circuit and will bank itself against one or other of the supply rails which requires a finite amount of time to recover from.

Integrator stage

Circuit elements U78 and U129 operate as an inverted, gated integrator. There are three operational states available for this circuit that are controlled by signals CDS_INTEGRATE and CDS_RESET – a). Idle, b). integrate, and c). reset. In the idle state both control switches are low and the feedback for U129 is just the integration capacitor C108. In this state the output of U129 is equal to the input signal magnitude multiplied by the inverted gain of 1 but since the input does not have a disturbing source (i.e. U78 switches 1 and 4 are off), whatever is on the output stays on the output as a steady potential (disregarding leakage effects through C108 and the switches of U78. This is the state used to hold the result of the correlated double sample operation and is later converted to a digital value.

In the integrate state, U78 switches 1 and 4 are connected to their respective outputs. This allows the input signal (TP42) to source current through resistors R245 and R250. The amplifier responds by trying to force charge into C108 to bring the inverting node of the amplifier back to the same potentials as the non-inverting node. Since the non-inverting node of U129 is held at ground potential through R233, the output of the amplifier tracks the non-inverting node input with an equal and opposite output voltage to force equal potentials on the input nodes. Whilst doing this the input is feeding current into the other side of the capacitor with a time constant equal to RC and a linear ramp is seen for a stable DC input signal potential. The unity gain time constant for the integrator approx. 660ns. i.e. the gain of the integrator is t/0.66 where t is the integration dwell time in microseconds. The integrator also has the function to limit the bandwidth of the signal after the integrator to approx 270KHz to reduce the white noise contribution.

After the integrator stage has sampled the detector reset level and pixel charge level and the output of the integrator has been sampled, the integrator must be reset to prepare for the next pixel process. This is achieved by setting U78 switches 2 and 3 on via signal CDS_RESET while switches 1 and 4 are off (CDS_INTEGRATE held low). The charge accumulated on C108 is discharged through the switches. The resistance of each switch is approx. 10 Ohms so the discharge time (to 18-bit accuracy) is approx. 60ns.

The switch U78 is wired so that the two control signals commutate two switches each which are wired 'back-to-back' this arrangement is used to cancel charge injection effects of the switch.

Offset injection and ADC buffer

The detector video signal is now fed to the summing network of R103A and R103B. This network adds the bias signal generated by U82 to allow positioning the DC operating point of the circuit into the optimum range of the input to the ADC converter. The video signal and the bias voltage are divided by a factor of 2 by this network and fed to the single ended to differential buffer amplifier U75. This amplifier has a gain of 2 (which compensates for the summing node) and generates two outputs from the magnitude of the input signal. For a positive input voltage (vin) the non-inverted output produces a signal that is twice the input magnitude (i.e. vin x 2) and the inverting output produces an output voltage that has a value of (vin x -2 + ref x 2). This function provides a signal that has twice the dynamic range of the original input signal at TP36 to enhance signal to noise figures of the ADC. You will observe that at zero (i.e. ground) input signal from the inverter stage (TP14) the non-inverting output will be at the same voltage as the offset voltage produced by U82. The inverted output will be at +5v minus the offset voltage produced by U82. As the integrator voltage increases the non-inverting output will also increase in a linear manner and the inverted output will decrease towards zero in a linear manner. This buffer amplifier has a high frequency gain roll off that is controlled by C314 to limit the bandwidth (approx. 2 MHz) to reduce white noise pass through.

Analog to digital converter

The reference generated by U132 is at 5.0v and is used by the ADC (U76) to set the input dynamic range. This same reference is divided by 2 by resistors R253A and R253B to produce the amplifier common mode voltage of 2.5v. Resistor R89 provides a telemetry pick off and C319 creates a filter to prevent noise from the telemetry PCB trace from affecting the reference circuit.

Resistors R93, R94 and capacitors C310, C316, and C615 provide a moderate amount of anti-aliasing filtering to reduce the amplitude of noise outside the Nyquist frequency (1/2 of the ADC sampling rate). This filter has a 3db low pass bandwidth of approx. 500KHz for both differential and common mode signal paths.

The ADC is low power, 18-bit differential input SAR converter with very good linearity and noise specifications. The input dynamic range on each signal input equals the reference voltage on pin 1. The ADC uses current distribution techniques to perform a conversion cycle that demands a very low impedance reference source. The reference is buffered by a large amount of capacitance (C313) to provide this low droop reference supply. Conversion is initiated when a positive transition is detected on U76 pin 6. The conversion cycle takes approximately 800ns to complete during which time the serial data output signal on pin 7 is high impedance and pulled high by resistor R436 (page 1). After the conversion is complete U76 pin 7 is pulled low to indicate that conversion is complete and that new data is available. This allows the LCB FPGA to sample the ADC output signal (via U100 – Page 1) to identify the end of conversion and begin serial transfer of the data. This is accomplished when the LCB FPGA generates a clock (nominally 40 MHz) on U110 pin 6 that clocks pin 8 of U76. This clock signal is used by the ADC to output 18-bits of information on the serial data output pins. This data is passed through U100, through the AFE gateway logic, and acquired and formatted via serial to parallel conversion to become the pixel data value. All active ADC devices are readout in parallel through the interface of U100 and the AFE gateway logic. The acquisition logic waits for all active

ADCs to indicate their end-of-conversion before beginning the acquisition cycle. The ADC device is powered by a 2.5v supply generated for each individual device by U131 to reduce crosstalk. The output buffers of the ADC are powered by the 3.3v logic supply of the AFE via pin 10 of U76.

ADC offset buffer

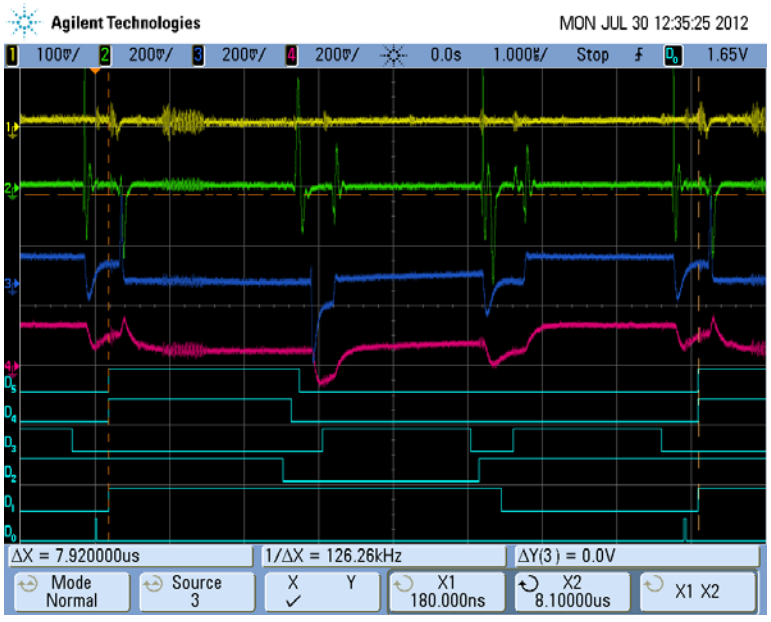
The ADC offset is controlled by amplifier U82 which accepts a unipolar input signal on the non-inverting input between 0 and 2.5v from DAC U92 (page 1) and voltage divider R241 and R240. The amplifier generates a bipolar output signal of +/- 5v that is divided by the video signal summing node of R103A and R103B to provide a +/-2.5v adjustment at the ADC. This corresponds to approx. half the dynamic range of the ADC. The frequency roll off of the offset amplifier is set to approx. 300 Hz by C302 to reduce noise contribution to the pixel data from this circuit.

CDS circuit gain

The overall gain of the AFE video processor circuit depends on the dwell time (i.e. integration time) used by the integrator during the CDS process. Using a 0.66us dwell time (for both the reset and video periods) results in unity gain for the processor. Under this condition 1 LSB of the ADC equates to 5v/2^18 volts / ADU (19.073uv/ADU). This would be the upper limit for the pixel rate at approx. 500 KPix/channel/sec. Considering a 200 KPix/channel/sec. rate, the dwell would more likely be of order 2us and the gain of the processor would be 2/0.66 i.e. 3.03 to give 6.3uv/ADU. These gains are multiplied by the gain of the TSM-PRE circuits. Using a 2us dwell time and requiring a conversion factor of 0.5 e-/ADU with a detector capable of delivering 5uv/e- would require a TSM-PRE gain of 2.5 (6.3 / 2.5) to be used.

CDS process timing

Figure 7 - CDS waveforms for zero input signal



Trace	Signal
D0	CNVTST - ADC Convert strobe
D1	INV – Signal inverted mode
D2	NONINV – Signal non-inverted mode
D3	INTEGRATE – Integrate signal
D4	DCRESTORE – Clamp input
D5	RESET – Reset integrator
Blue	TP36 – Integrator output
Yellow	TP40 – Input buffer signal
Red	TP41 – ADC positive input
Green	TP42 – Invert / Non-invert amplifier

Figure 8 - CDS waveforms for simulated input signal

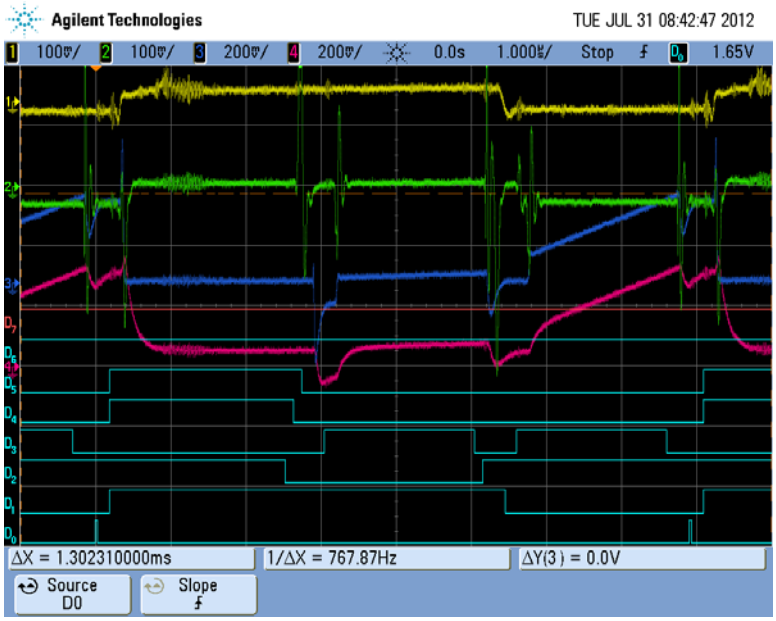


Figure 1 shows a normal CDS process cycle for one pixel with zero signal. Figure 2 shows the same waveform with a simulated detector output signal. The process begins with the integrator reset control signal (D5) and DC clamp control signal (D4) true during the detector reset period. This normalizes the circuit for processing the video signal and isolates the input buffer from any large transients from detector reset clock feed through. During this period the invert/non-invert amplifier is also held clamped by setting the invert and non-invert control signals true (D1 and D2). The circuit comes out of reset and the switched to inverting mode just before the first integration period (dwell period) occurs on D3. This integration period corresponds to the sample of the reset potential of the detector output. You can see that there is a slight DC offset in the circuit that is visible as the increase in the integrator and ADC buffer outputs (blue and red traces). After the first integration period (2us in this example), the integrator control signal is taken low and the signal converted to non-inverting mode by the sequence of control signals apparent on D1 and D2. This normally occurs simultaneously with the switching of the detector summing well clock to dump the pixel charge onto the sense node in the detector. This has the effect (in an N-Channel detector) of reducing the voltage at the detector amplifier output. After this the integrator is again enabled (D3) for the same dwell time to compute the difference between the reset and pixel levels of the detector. In this example, no charge is dumped and the detector amplifier output level remains unchanged (i.e. at bias level). The integrator now ramps down for the same DC offset voltage effect and terminates after 2us. A short delay is given to let the integrator output and ADC buffer amplifier settle before the result is converted when the ADC convert signal (D0) goes high. Note that the integrator produces an inverted output (i.e. the integrator gain has a negative sign) so the sequence of signal processing - inverted then non-inverted - produces a positive output response of the integrator for an increase in electrons in the detector pixel (again for N-Channel detectors).

There are obvious offsets and transients produced in the circuit during the eleven steps of the CDS process. These are the products of finite parasitic capacitance and control signal feed through in the circuit elements. The essence of the ability of the circuit to produce low noise data is that these offsets and transients are the same amplitude and phase for each pixel. Under this condition, the overall effect

is to reduce the offsets and transients to a constant DC offset in the value computed for each pixel that does not contribute to the noise of the detector signal.

Note that there is approximately 180ns delay between the activation of a CDS control signal and the effect on the analog signal process. This is produced by the finite turn-on and turn-off times of the respective analog switches and the response time of the amplifiers and is normal.

5.8 Telemetry Circuits.

Refer to schematic TRNT-EL-04-2004, page 2.

Extensive telemetry facilities are provided to assist in diagnostics of the hardware of the Torrent DHE before removing the controller form service i.e. the telemetry is meant to be used as the first line diagnostic facility. The AFE provides for telemetry on all power supply and reference circuits for this reason.

Clock, bias, power and reference telemetry

Two 32 channel analog multiplexors (U40 and U66) are used to commutate the respective telemetry pick offs to feed a low power 2-channel 12-bit ADC device (U144). The multiplexors are controlled by the same serial data control signals as the DAC devices (DAC_SCLK, DAC_SDIN, and /TELMUXn_SYNC). All signals at the inputs to the multiplexor have a dynamic range of 5 volts. For signals that are bipolar in nature (i.e. clocks and biases) and for the negative supply voltages, resistor networks are used to offset the input voltage to the multiplexor.

The outputs of each multiplexor are buffered by amplifiers configured as voltage followers (U145, U134) to present a low impedance drive to the ADC device inputs. The ADC has two multiplexed inputs that are controlled by the telemetry serial data control signals TEL_SCLK, TELADC_DIN, and /TELADCn_SYNC signals. Conversion of the telemetry values is accomplished by sending a 16-bit serial command to the ADC which sets the required channel and initiates a conversion. This conversion process is timed by the same TEL_SCLK as the serial data transmission and results in a 12-bit result after sixteen more clock periods. The result is then readout through the AFE interface (U100) in sixteen clock periods on U144 pin 1 while the next channel is being converted by the ADC.

The telemetry control firmware in the LCB FPGA device scans these channels periodically to place the values into attribute registers. The time required to read all telemetry is approx. 1.3ms and TEL_SCLK is run at 5MHz. The period between telemetry scans is controlled by the **TelScanInt** attribute and is normally set to 1000ms between scans. Telemetry scans are normally switched off by the sequence during detector readout to prevent asynchronous processes injecting noise into the pixel data.

DAC telemetry channels

There are four other channels of telemetry available through ADC converters U57 and U139. These channels use the analog multiplexor built into the DAC devices to sample the output of the DAC channels before the DAC output amplifier. Their values will show half the DAC output value and serve to confirm correct setting and operation of the DAC devies themselves. This telemetry can be accesses by switching off periodic scanning (i.e. set **TelScanInt** to zero) and sending commands to address and read groups of DAC channels using the **TelScanCmd** attribute (see the Firmware Users Guide for more information on these attributes).

Note that when appropriate, all telemetry ADC devices are read out simultaneously and in parallel i.e. when more than one group is specified in the **TelScanCmd** attribute, the serial command data to the converters and the data transfer from the converters occur on all signal channels simultaneously.

5.9 Test Points.

Refer to schematic TRNT-EL-04-2004, page 1.

There are eight test points available to test clock and bias signals generated by the AFE board. These signals are available on JT2 and JT3 that are mounted close to the flex cable connectors of the AFE board. The test point multiplexors are built from analog switches and addressable latches controlled using the LCB FPGA device. Each time a new value is written to one of the Afe1/2TpClkn, Afe1/2TpLvbiasn, or Afe1/2TpHvbiasn attributes a new address is generated and sent to the latches U2, U3, U64, or U68 (depending on which attribute was written to). The latch outputs enable or disable the relevant analog switch to pass the signal to the test point connectors. Each analog switch (U4 => U7, U59, U60, U71, U73) and buffer amplifiers (U1A/B, U152A/B, U136A/B, U137A/B) receive power from the power supply that corresponds to its signal function group. The test points sample their signals from the controller side of the signal i.e. before the detector isolation switches. This allows you to test clock and bias signals without applying the voltage to the detector and to determine any change in the voltages due to detector loading or faults downstream of the controller.

5.10 I2C Interface Circuits.

Refer to schematic TRNT-EL-04-2004, page 11.

Each physical circuit board in the Torrent DHE must present a standard I2C interface with predefined devices to the LCB to enable board identification and system connectivity processes to be carried out. The presence of an I2C bus indicates that the hardware module is present and can be used. The presence test requires that there be three wires associated with the I2C bus. These are a standard serial clock used for synchronous data transmission called SCLK, a data input or source wire called AFE_SDA_SRC, and a data output or sense wire called AFE_SDA_SNS. The AFE_SDA_SRC and AFE_SDA_SNS wires are connected on the interface via an 825 Ohm resistor. The LCB uses this connectivity to allow it to poll the interface and establish presence. This connectivity scheme also allows the use of a remote power source (AFE_SDA_SRC) for the pull up resistor (R62) when data is transmitted from a slave device to the LCB I2C master controller. The standard devices and their logical address are listed in Table 18.

Table 18 - Standard I2C Bus Device Assignments

Circuit Designation	Device	Purpose	Interface Address
U72	DS28CM00	Silicon serial number to uniquely identify the hardware. Telemetry shows this as afe1(2)SerialNum.	0x50
U140	24AA128	4096 x 32-bit EEPROM to store calibration coefficients for the hardware.	0x54
U151	MCP9803	Local temperature sensor for DHE monitoring. Telemetry shows this as	0x48

		afe1(2)Temperature1.	
U70	MCP9803	Local temperature sensor for DHE monitoring. Telemetry shows this as afe1(2)Temperature2.	0x49

Power for these circuits is derived from the interface supply (VPIFC) so the I2C bus can be accessed without applying analog power to the AFE board.

6.0 Video Flex Circuit (FLEX-VID)

Refer to schematic TRNT-EL-04-2005.

This description corresponds to Revision –A– of the hardware.

The small flexible circuit provides the connection between the TSM_PRE video signal preamp outputs and the AFE video input stage through the Controller module to Transition module mechanical interface. This flex circuit also carries the power and grounding network for the TSM-PRE preamplifier power supplies. The flex circuit is split to provide separate power, video signal, and ground connections to each AFE board in order to avoid ground loops and interference for occurring. There are also two separate shield connections that are undedicated and can be used to connect to video cable shields if required. There are no active components on the video flex circuit. Be careful when inserting the flex circuits connectors into the AFE board connectors. The connector type will allow you to mate the connectors when they are offset by one connector row which will cause a fault that is hard to diagnose.

7.0 Clock and Bias Flex Circuit (FLEX-CB)

Refer to schematic TRNT-EL-04-2006.

This description corresponds to Revision –A– of the hardware.

The wide flexible circuit is used to connect the AFE outputs of the clock and bias signals to the TSM-PRE board through the Controller module to Transition module mechanical interface. Separate bias and clock returns are provided to avoid ground loops and interference for occurring. This isolation between AFE boards is carried through the circuitry on the TSM-PRE clock an bias conditioning circuits so that they can be connected at the detector if so desired. There are no active components on the video flex circuit. Be careful when inserting the flex circuits connectors into the AFE board connectors. The connector type will allow you to mate the connectors when they are offset by one connector row which will cause a fault that is hard to diagnose.

8.0 Transition Module Preamp (TSM-PRE)

Refer to schematic TRNT-EL-04-2007.

This description corresponds to Revision –B– of the hardware.

The component references used in this description apply to AFE 1, channel 1 however, the operation and topography of each channel is identical.

The TSM-PRE module provides the means to:

1. Amplify the detector video signal to achieve the correct signal conversion factor.
2. Provide resistive loads for the detector amplifier source outputs
3. Allow optional clock shaping and hardware protection for inverted polarity.
4. Allow optional bias supply filtering and hardware protection for inverted polarity
5. Provide for connecting wires to the detector Dewar connectors
6. Provide a detector substrate safety ground when the Controller is removed from the Transition module.

Preamplifier circuits.

The four preamplifiers for each AFE are on separate circuits to prevent ground loops and crosstalk from occurring. The group of four amplifiers are powered from a bipolar power supply derived through U11 and U9. These devices are fed from separate +/-10v supplies originating on the respective AFE board through connector pins 44 and 42 respectively. The regulated output is normally +5.5v and -5v. If the amplifier type used for the preamplifier is substituted these regulators may be adjusted by changing resistors R238 and R122 so as to provide alternate preamplifier power supplies.

The detector amplifier source output is loaded by R88. This resistor should be changed for different applications to suit the appropriate quiescent current for the detector. Capacitor C22 provides the AC coupling function to DC shift the video signal input into the common mode signal range of the preamplifier U8. R24 provides a return path for the input leakage current of the amplifier and R22 balances the impedance seen by the leakage across the two input nodes of the amplifier. C135 provides the inverting input node parasitic capacitance compensation to help stabilize the amplifier feedback circuit. The feedback circuit comprises of resistors R86, R23, and C76 which normally provide a gain of 2.3 with a bandwidth of 5MHz. This is sufficient bandwidth for operating detectors up to approx. 250KPix/sec with output sensitivities of 5uv/e- to achieve 18-bit precision at ½ e-/ADU.

At this gain the nominal noise figure for the complete signal chain is 3.6 ADU rms which equates to 1.8 e-. With a detector that has a 3e- rms noise figure this will provide for a total read noise of 3.5 e- rms for this detector (i.e. the controller will contribute 0.5e- of noise signal).

The output signal from the preamplifier and the gain reference (ground) of each amplifier are sent to the AFE via J1 and then through the video flex circuits to the appropriate AFE. The arrangement of sending the ground reference back to the input stage of the AFE is compatible with the PCB layout of the AFE where each video signal processor circuit has its own isolated ground plane that connects back to the common ground plane under the Analog to digital converter.

Clock circuits.

Each clock signal has a series resistor (R89) and capacitor shunt (C91) pair associated with it. These can be used to shape the clock waveform edges to slow them down and / or to filter out high frequency noise. Additionally these reserved component pads can be used to fit protection diodes to prevent reverse polarity signals from damaging the detector (for example, for CMOS devices). The clock signals are brought out to a pair of through hole solder pads on J6 that are designed to receive point-to-point wiring to connect the clock signals to the detector Dewar connectors.
Separate clock returns are provided to route clock currents to the appropriate AFE board (i.e. back to the AFE that is sourcing the clock signals).

High voltage bias circuits.

Each high voltage bias signal has the provision to implement RC filtering (R104, C104) and to install a reverse polarity protection diode (D1:C). The high voltage signals are brought out to a pair of through hole solder pads on J7 that are designed to receive point-to-point wiring to connect the high voltage bias signals to the detector Dewar connectors. Separate high voltage bias returns are provided to route currents back to the appropriate AFE board (i.e. back to the AFE that is sourcing the high voltage bias signals).

Bias circuits.

These circuits are very similar to the clock circuit type. Each bias circuit has a series resistor (R100) and capacitor shunt (C87) pair associated with it. These can be used to filter out high frequency noise and reduce the effective impedance of the signal when a long cable is used. Additionally these reserved component pads can be used to fit protection diodes to prevent reverse polarity signals from damaging the detector. The bias signals are brought out to a pair of through hole solder pads on J8 that are designed to receive point-to-point wiring to connect the clock signals to the detector Dewar connectors. Separate bias returns are provided to route bias currents back to the appropriate AFE board (i.e. back to the AFE that is sourcing the bias signal).

9.0 Transition Module Utility (TSM-UTIL)

Refer to schematic TRNT-EL-04-2009.

This description corresponds to Revision –A2– of the hardware.

9.1 Introduction

The transition module utility board acts as an interface between detector-specific implementation for temperature control and a standard DHE Controller module. The interface conditions the temperature sensor inputs from a typical detector dewar implementation and provides a calibrated output to the temperature controller implemented on the LCB. This is achieved by converting the typical high impedance voltage difference signal seen across the sensor to a frequency proportional to temperature. The board contains two identical temperature sensor conditioning circuits, a standard I2C interface to detect the presence, status and serial number of the utility board, a small eeprom store for detector coefficients, and feed-through traces for shutter control, shutter status and preflash control.

9.2 Temperature Sensor Conditioning Circuit

Referenced to drawing TRNT-EL-04-2009, page 1.

Each temperature sensor conditioning circuit is identical. The following description will use the component designations of channel one to describe the circuit but these descriptions apply equally to channel two.

The circuit is designed to support both Si diode and PT100 type sensors. A current source is provided by an LM337 device (U6) that is programmed by resistors R22 and R24 to supply a 10μa source current. U6 is temperature stabilized by adding the reverse temperature coefficient of U6 generated by D1. The amount of temperature stabilization added to the feedback on U6 pin 1 is adjusted by the ration of the two current set resistors. A table is shown on the schematic to identify normal values of these resistors for the two types of sensor.

R37 to R44 are provides to strap the current sources to the input section of the temperature sensing circuits when a two-wire sensing configuration is used. The table on the schematic also provides details for these resistors. Zero ohm 0805 format resistors are used to provide the strapping.

R25 to R28 together with C19, C20, C23, C24 provide buffering and to the sensor source and the return signals to float the detected potential difference of the sensor between the ground and power supply to put the sensors potential difference inside the common mode range of the sensor input amplifier U3:B.

The sensor input amplifier (U3:B) will amplify the difference signal from the sensor and add an offset for setting a zero point on the slope of the transfer function. The nominal gain for a silicon diode temperature sensor will be 4.76 that makes the transfer function slope equal to10mv per degree Kelvin. The gain is adjusted by RV4.

A typical silicon diode implementation will exhibit approximately 380mv of offset at room temperature and at 10μa current. This offset has to be calibrated to give an absolute temperature reference point. This is achieved by setting the diode to a known temperature and adjusting RV5 to make the voltage at TP1 test point equal to the temperature in Kelvin divided by 100. For example, at a diode temperature of 77K with the diode submerged in a LN2 bath, the voltage on TP1 test point should be adjusted using RV5 to be 770mv.

The output of the sensor input amplifier is lightly filtered by R3 and C4 and fed to the control input of a voltage to frequency converter represented by U4. This device accepts an analog input signal to control a free running oscillator whose frequency is proportional to the input signal. The proportionality is calibrated by RV3 and designed to provide a 50Hz change of frequency for each millivolt of control signal. This is equivalent to 500Hz per degree temperature change after the gain of the sensor input amplifier. For example, at a sensor temperature of 77 Kelvin, TP1 must show 770mv and the TEMP_1 signal should measure 38.5KHz.

U4 has an open collector output stage on pin 1 that is routed back to the LCB via connector P1 pin 9 and a dedicated trace on the PSM to the LCB power supply connector. The LCB provides the pull-up for the U4 output stage and buffers the signal before measuring the frequency in the FPGA.

The temperature conditioning circuits are powered from a small 12 Volt linear regulator mounted in the PSM that provides a clean power source via connector P1 pin 13.

9.3 Calibration Procedure for Temperature Sensor Conditioner Circuits

Silicon Diode and PT100 Sensors

1. Connect a waveform generator to across a silicon diode appropriately connected to a temperature sensor channel. Set the waveform generator for 10 KHz square wave at 200mv pk-pk output. You may have to use a 50 Ohm shunt load to get a stable and exact waveform.
2. Connect an oscilloscope to TP1 and adjust RV4 to obtain 952mv pk-pk modulation (200mv x 4.76 nominal gain).
3. Disconnect the waveform generator.
4. Set the diode temperature to be stable at 77K in a LN2 bath. Adjust RV5 for 770mv at TP1.
5. Connect the oscilloscope to TP4 and adjust RV3 to obtain 38.5KHz (77K x 500Hz/deg.) TP1 should read 770mv.
6. Set the diode temperature to be stable at 273K (in an ice bath). Tweak RV4 to obtain 136.5KHz at TP4 (273K x 500Hz/deg.). TP1 should read 2.73 Volts.
7. Once again, set the diode temperature to be stable at 77K in a LN2 bath and check for 38.5KHz at TP4. Tweak if necessary.

These calibration steps should provide the best possible linear range across the operating temperature of a normal CCD. It is possible to use additional tweak steps to improve the absolute accuracy or to use different set temperatures on the diode to optimize a different range of temperatures. The dynamic range of the interface is approximately 4.5 Volts at TP1, which is equivalent to 450 Degrees Kelvin.

9.4 I2C Interface Circuit Description

Each physical circuit board in the Torrent DHE must present a standard I2C interface with predefined devices to the LCB to enable board identification and system connectivity processes to be carried out. The presence of an I2C bus indicates that the hardware module is present and can be used. The presence test requires that there be three wires associated with the I2C bus. These are a standard serial clock used for synchronous data transmission called SCLK, a data input or source wire called SDA_SRC, and a data output or sense wire called SDA_SNS. The SDA_SRC and SDA_SNS wires are connected on the interface via an 825 Ohm resistor. The LCB uses this connectivity to allow it to poll the interface and establish presence. This connectivity scheme also allows the use of a remote

power source (SDA_SRC)for the pull up resistor (R1) when data is transmitted from a slave device to the LCB I2C master controller. In addition to the normal compliment of I2C devices, the TSM-UTIL board carries an additional device used to measure the VBB potential.

The standard and Vbb Telemetery device and their logical address are listed in Table 19.

Table 19 - TSM-UTIL I2C Bus Device Assignments

Circuit Designation	Device	Purpose	Interface Address
U1	DS28CM00	Silicon serial number to uniquely identify the hardware. Telemetry shows this as tsmSiliconSerialNum.	0x50
U2	24AA128	4096 x 32-bit EEPROM to store detector coefficients and system identification with the detector dewar.	0x54
U9	MCP9803	Local temperature sensor for DHE monitoring. Telemetry shows this as tsmTemperature1.	0x48
U8	MCP9803	Local temperature sensor for DHE monitoring. Telemetry shows this as tsmTemperature2.	0x49
U13	LTC2301	Analog to digital converter used to sense Vbb Telemetry.	0x08

Power is derived from the VP12 supply via a small local regulator (U11, R15, R16) that develops 3.3V specifically for these devices.

9.5 Detector Heater Power Limit Selection

R17, R18, R19, and R20 are used to establish a maximum heater power that the heater supply in the PSM can develop into a resistive heater element in a detector dewar. The selection is made by appropriate strapping of the resistors across the signals VHTR_LIMIT_P and VHTR_LIMIT_N by switch SW1. Table 20 shows the appropriate selection for heater power limiting. The values assume a 35 Ohm resistive heater element for power calculation.

Table 20 - Detector Heater Power Limit Options

Jumper Position	Resistor Value	Maximum Power	Maximum Current
OPEN	Infinity	8.75 Watts	0.5 Amps
JP4	220K-Ohms	3.68 Watts	0.324 Amps
JP3	120K-Ohms	1.77 Watts	0.225 Amps
JP2	44.2K-Ohms	0.830 Watts	0.154 Amps
JP1	0-Ohms	0.5 Watts	0.125 Amps

9.6 Chassis Ground Continuity

Since the DHE Controller Module can be physically removed from the TSM the chassis ground is carried through connector P1 pin 11 on the utility board to assure connectivity between these two mechanical components.

A separate (uncontaminated) shield wire is available on solder pad E8 of the TSM-UTIL board. This provides a means to connect the Dewar housing (or anything else for that matter) directly to the remote power and ground connector chassis ground pin without passing through other circuit areas.

9.7 Utility Feed-through Signals

Several signals generated by the PSM and/or sensed by the LCB are fed through connector P1 to become available for connection via J2. These are to control and monitor the shutter and preflash facilities. The command signas **SHUTTER_OPEN** and **PREFLASH_ON** are open collector outputs, low true and common to the **SHUTTER_RTN** signal. They are intended to be used to control a shutter mechanism and perhaps a calibration source inside a dewar. The four signals **SHUTTER_SENSE_OPEN_P, SHUTTER_SENSE_OPEN_N, SHUTTER_SENSE_CLOSED_P** and **SHUTTER_SENSE_CLOSED_N** are two pairs of uncommitted inputs to opto-isolator devices on the PSM. They should be driven by a 5ma current source (or equivalent) to indicate the mechanical position of a shutter.

Solder pads E12 – E15 provide connection areas for the detector heater supply.

9.8 VBB Feed-through, filter and telemetry circuit

The purpose of this circuit is to remove any remnant noise from the VBB supply and provide feedback of the actual potential to the servo that controls the PSM power supply circuit. Capacitors C35 – C37 and resistors R30 and R31 form an RC filter to remove ripple and noise from the back-side potential (VBB) produced by the PSM. The VBB_RTN signal used to support the filter on an isolated ground reference also generated from the PSM. The VBB supply is available on an SMA connector (J3) mounted to the TSM_UTIL board. The resistive divider formed by R32/R33 is used to condition the VBB potential to the dynamic range of the analog to digital converter represented by U13. This device operates in bipolar mode to produce the feedback telemetry for the supply that is used to servo the supply. The ADC is power from a 5v supply generated by U12. It is included in the I2C communications of the TSM-UTIL I2C bus. Note that C35 is normally not populated to reduce the capacitive loading on the VBB amplifier and so improve the stability.

10.0 Dewar Connector Plate (DCP)

Refer to mechanical drawing TRNT-EL-02-1022.

This description corresponds to Revision –B– of the hardware.

The isolated connector plate is provided to mount the connectors that mate to the hermetic connectors mounted at the vacuum interface of the Dewar. The plate is built from FR4 material to provide galvanic isolation of the TSM module and Dewar. This allows for independent configurations of the Dewar and Torrent controller grounding schemes suitable for every individual application of Torrent. The plate has been designed to accommodate 'standard' connector mounting configurations for the KPNO and CTIO Dewar systems. Note that the mechanical TSM module itself can be modified to provide alternate mounting arrangements e.g. using the TSM access panel to mount the Dewar mating connectors to provide a vertical mounting configuration. In the standard configuration the mating connectors are solder cup cable types (e.g. Amphenol PT02A-20-41P) which are mounted using a jam nut to secure them and provide a margin of lateral movement to accommodate mechanical tolerances of the Dewar. The connectors are then wired point-to-point using the available thru-holes on the TSM-PRE board to connect the relevant signals to the detector via the connectors.

Appendix I Power Supply Synchronization Frequencies

This document (Power Supply Sync Analysis.xls) is also available from this source

Table 21 - Range of Power Supply Synchronization

Supply	Min KHz	Max KHz
VP33D_SYNC	300	600
V80A_SYNC	660	1000
V300A_SYNC	125	250
VLOGIC_SYNC	750	2250

Pixel Rate	f /2	f	f x 2	f x 3	f x 4	f x 6	f x 8
	KHz	KHz	KHz	KHz	KHz	KHz	KHz
		50.000		150.000		300.000	
		60.000		180.000		360.000	
		70.000		210.000		420.000	
		80.000	160.000	240.000		480.000	
		90.000	180.000			540.000	720.000
		100.000	200.000	300.000		600.000	800.000
		110.000	220.000	330.000		660.000	880.000
		120.000	240.000	360.000		720.000	960.000
		125.000	250.000	375.000		750.000	1000.000
		130.000		390.000		780.000	1040.000
		140.000		420.000		840.000	1120.000
		150.000	300.000	450.000		900.000	1200.000
		160.000	320.000			960.000	1280.000
		165.000	330.000		660.000	990.000	1320.000
		170.000	340.000		680.000	1020.000	1360.000
		180.000	360.000		720.000	1080.000	
		190.000	380.000		760.000	1140.000	
		200.000	400.000		800.000	1200.000	
		210.000	420.000		840.000	1260.000	
		220.000	440.000		880.000	1320.000	
		230.000	460.000		920.000	1380.000	
		240.000	480.000		960.000	1440.000	
	125.000	250.000	500.000	750.000	1000.000	1500.000	
	130.000	260.000	520.000	780.000	1040.000	1560.000	
	135.000	270.000	540.000	810.000	1080.000		
Default	140.000	280.000	560.000	840.000	1120.000		
	145.000	290.000	580.000	870.000	1160.000		
	150.000	300.000	600.000	900.000	1200.000		
	155.000	310.000		930.000	1240.000		
	160.000	320.000		960.000	1280.000		
	165.000	330.000	660.000	990.000	1320.000		

Pixel Rate	f /2	f	f x 2	f x 3	f x 4	f x 6	f x 8
	170.000	340.000	680.000	1020.000	1360.000		
	175.000	350.000	700.000	1050.000			
	180.000	360.000	720.000	1080.000			
	185.000	370.000	740.000	1110.000			
	190.000	380.000	760.000	1140.000			
	195.000	390.000	780.000	1170.000			
	200.000	400.000	800.000	1200.000			
	205.000	410.000	820.000	1230.000			
	210.000	420.000	840.000	1260.000			
	215.000	430.000	860.000	1290.000			
	220.000	440.000	880.000	1320.000			
	225.000	450.000	900.000	1350.000			
	230.000	460.000	920.000	1380.000			
	235.000	470.000	940.000	1410.000			
	240.000	480.000	960.000	1440.000			
	245.000	490.000	980.000	1470.000			
	250.000	500.000	1000.000	1500.000			

Appendix II LED_1_Slct and LED_2_Slct Indicator Attributes

There are two 8-bit registers assigned to provide visual indication of the internal signals of the FPGA. These registers are read / write. By setting a bit true the indicator (LED1 or LED2) will flash briefly (25ms) every time the selected signal becomes active true. LED1 is currently mounted on the Sync In port connector and LED2 is mounted on the Sync Out Port connector. The tables below indicate the significance of each attribute bit.

Table 22 - Led1_Slct Attribute – J8 – Top RJ45 connector

LED1 Signal Select Bits	
bit	**signal**
7	**BUSRESET**
6	**SLAVEERROUT(4)**
5	**SLAVEERROUT(3)**
4	**SLAVEERROUT(2)**
3	**SLAVEERROUT(1)**
2	**SLAVEERROUT(0)**
1	**CFGCYCLEREQUEST**
0	**LCBCYCREQUEST**

Table 23 - Led2_Slct Attribute – J9 – Bottom RJ45 connector

LED2 Signal Select Bits	
bit	**signal**
7	**SRC_SYNC_OUT**
6	**SNK_SYNC_IN**
5	**V33_SYNC_OUT**
4	**V300_POLARITY**
3	**V180_PWR_EN_N**
2	**V80_PWR_EN_N**
1	**VFAN_PWR_EN_N**
0	**MCLK_SEL_N**

Appendix III FPGA Debug Signal Multiplexor Assignments

This attribute controls the selection of a group of eight signals that are presented on the CFGDATA(7:0) signals (connector J4) on the LCB. By setting the attribute to different values, the hardware debug signals are available for diagnostic use. The attribute accepts values from zero to ten. The list below shows the significance.

Table 24 - DbgSigSlct Attribute Values

DbgSigSlct Attribute Values	
Value	**Signal Group**
0	Signals off
1	LCB Control Signal group
2	PSM Services Signal group
3	CFG Services Signal group
4	PIX Services Signal group
5	AFE Control Signal group
6	Signals off - Future AFE2 Signal group
7	Signals off - Spare
8	CLK Services Signal group
9	System Bus Signal group
10	Auxiliary Signal group

The following tables list the individual signals for each group.

DbgSigSlct = 1 - LCB Services Signal Assignments	
bit	**signal**
7	**FPDPDATAOUTRDY**
6	**FPDPDATAOUTACK**
5	**FPDPDATAINRDY**
4	**FPDPDATAINACK**
3	**GIGEDATAOUTRDY**
2	**GIGEDATAOUTACK**
1	**GIGEDATAINRDY**
0	**GIGEDATAINACK**

DbgSigSlct = 2 - PSM Services Signal Assignments	
bit	**signal**
7	**MEM_PWR_ENBL**
6	**TEMP_1_SNS**
5	**SEQ_SYNC_CLK**
4	**LOGIC_SYNC**

3	**V300_SYNC**
2	**V180_SYNC**
1	**V80_SYNC**
0	**V33_SYNC**

DbgSigSlct = 3 - CFG Services Signal Assignments

bit	signal
7	**SEQDBGSIGS(0) - WBWRTREQ**
6	**SEQDBGSIGS(1) - WBWRTACK**
5	**SEQDBGSIGS(2) - SEQDBG_0 - RUN**
4	**SEQDBGSIGS(3) - SEQDBG_1 - BUSREQUEST**
3	**STARTEXPOSURE**
2	**I2C_RDERR(0)**
1	**I2C_BUSY**
0	**I2CRDCMD**

DbgSigSlct = 4 - PIX Services Signal Assignments

bit	signal
7	**WBWRTENABLE**
6	**WBSTATUSOUT(1)**
5	**WBSTATUSOUT(8)**
4	**WBSTATUSOUT(3)**
3	**MEMPWRENABLED**
2	**RESET**
1	**DLYCLOCKLOCKED**
0	**PHY_INIT_DONE**

DbgSigSlct = 5 - AFE Control Signal Assignments

bit	signal
7	AFE_PWRDATA(68) - Data Enable
6	AFE_PWRDATA(64) - Data Clock
5	AFE_PWRDATA(64) - ADC Clock
4	AFE_PWRDATA(0) - ADC(0) SDOUT
3	StreamLineStart
2	StreamFrameStart
1	StreamDataReady
0	StreamDataClk

DbgSigSlct = 8 - CLK Services Signal Assignments

bit	signal
7	**DCLK_FEED**

6	**SYNC_IN_CLK_FEED**
5	**MCLK_SEL_N**
4	**CLK_LOOP_LOCK**
3	**CLK_CTRL_SYNC**
2	**CLK_CTRL_CS_N**
1	**CLK_CTRL_DATA**
0	**CLK_CTRL_CLK**

DbgSigSlct = 9 - System Signal Assignments

bit	signal
7	**MSTR1GRNT**
6	**MSTR0GRNT**
5	**SLAVECYCLE**
4	**SLAVEWRITE**
3	**SLAVEERROR**
2	**STATUSENABLE**
1	**SLAVEACK1**
0	**SLAVEACK0**

Appendix IV Torrent Attribute List

This document (TRNT-AD-08-0010) can be found here