# NOAO

## ENGINEERING CHANGE ORDER



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|---|---|---|---|---|---|---|---|
| BOARD NAME | TORRENT CCD PREAMP TRANSITION | | | ECO# | **TRNT-40** | DATE | 19/07/16 |
| BRD SERL# | 31 | REV | | ART# | | | |
| PN# | TRNT-EL-04-1007 | REV | C | | | REV | |
| ASBLY# | | REV | | PCB# | TRNT-EL-04-2007 | REV | C1 |
| BOM# | | REV | | SCH# | TRNT-EL-04-2007 | REV | C1 |
| COGNIZANT ENGNR | Peter Moore & Braulio Cancino | | | CHARGE# | | | |

REASON FOR MODIFICATION:

Special Pre-Amp for 0.9m Tek – 2k.

Optimize frequency response of the input filter, input impedance and low-pass filter of clock signals.

| DRAWINGS AFFECTED: | NEW REV |
|---|---|
| TRNT-EL-04-2007 | C1 |

DESCRIPTION OF MODIFICATION:

1. Change: C24 = C23 = C18 = C21 = 5.6 nF – Increased bandwidth by decreasing the input low pole frequency.
2. Change: R71 = R68 = R64 = R60 = 8 kΩ – Decreased input impedance.
3. Change: R12 = R9 = R6 = R3 = 220 kΩ - Increased bandwidth by decreasing the input low pole frequency.
4. Change: C73 = C71 = C70 = C69 = 120 pF – Decreased bandwidth by decreasing the input high pole frequency.
5. Change: R91 = R115 = R92 = R116 = R94 = R118 = R90 = R114 = R27 = R52 = R26 = R51 = R31 = R54 = R28 = R50 = 300Ω. (1C4 – 1C6 – 1C8 – 1C2 – 1C5 – 1C7 – 1C9 – 1C3; 2C4 – 2C6 – 2C8 – 2C2 – 2C5 – 2C7 – 2C9 – 2C3) – Low-Pass filter serial and summing well clocks.
6. Change: C97 = C92 = C98 = C99 = C35 = C34 = C41 = C40 = C109 = C116 = C111 = C108 = C59 = C54 = C55 = C53 = 200 pF. (1C4 – 1C6 – 1C8 – 1C2 – 1C5 – 1C7 – 1C9 – 1C3; 2C4 – 2C6 – 2C8 – 2C2 – 2C5 – 2C7 – 2C9 – 2C3) – Low-Pass filter serial and summing well clocks.
7. Change: R95 = R29 = R30 = R32 = R117 = R53 = R55 = R56 = 60Ω. (1C10 – 1C11 – 1C13 – 1C15; 2C10 – 2C11 – 2C13 – 2C15) - Low-Pass filter parallel and transfer gates clocks.
8. Change: C90 = C42 = C36 = C37 = C110 = C56 = C113 = C57 = 1nF. (1C10 – 1C11 – 1C13 – 1C15; 2C10 – 2C11 – 2C13 – 2C15) - Low-Pass filter parallel and transfer gates clocks.

9. Change: R89 = R25 = R113 = R49 = 250Ω (1C0 – 1C1; 2C0 – 2C1). Low-Pass filter reset gate clocks.