

NOAO

ENGINEERING CHANGE ORDER

BOARD NAME <u>TORRENT Local Control Board (LCB)</u>	ECO# TRNT-039	DATE <u>8/07/2014</u>
BRD SERL# <u>ALL</u> REV _____	ART# _____	
PN# _____ REV _____	REV _____	
ASBLY# <u>TRNT-EL-04-0002</u> REV <u>B</u>	PCB# _____	REV _____
BOM# <u>TRNT-EL-04-4002</u> REV <u>B</u>	SCH# <u>TRNT-EL-04-2002</u>	REV <u>B</u>
COGNIZANT ENGR <u>Peter Moore</u>	CHARGE# _____	

REASON FOR MODIFICATION:

1. Decrease system clock jitter by optimizing the clock generator PLL loop filter (U28).

DRAWINGS AFFECTED:	NEW REV
TRNT-EL-04-2002 B	B1

DESCRIPTION OF MODIFICATION:

1. Change C254 from 10nF to 1.5nF
2. Change C255 from 5.6nF to 15pF
3. Change R254 from 3.65K Ohms to 2.74K

See new TI data sheet - <http://www.ti.com/product/lmk03000?keyMatch=lmk03000&tisearch=Search-EN>

The newer TI data sheet provides corrected information for the device relative to the original National Instruments version of the data sheet.

New code block for firmware download (Torrent_FPGA_V224 and later) provides for the R3/C3 & R4/C4 settings and a change in the CP Gain value.