NOAO

ENGINEERING CHANGE ORDER

BOARD NAME	TORRENT CCD AFE			ECO#	**TRNT-019**	DATE	03MAY2011
BRD SERL#	010 >	REV		ART#	TRNT-EL-07-0004		
PN#		REV				REV	
ASBLY#	TRNT-EL-04-0004	REV	A	PCB#	TRNT-EL-04-1004	REV	A
BOM#	TRNT-EL-04-4004	REV	A	SCH#	TRNT-EL-04-2004	REV	A
COGNIZANT ENGNR				APPROVD			

REASON FOR MODIFICATION:

DRAWINGS AFFECTED:	NEW REV
TRNT-EL-04-0004	B
TRNT-EL-04-1004	B
TRNT-EL-04-2004	B
TRNT-EL-04-3004	B
TRNT-EL-04-4004	B

DESCRIPTION OF MODIFICATION:

1. more space between U145 and R47
2. inductors L1 & L2 move away from card edge .125-.250 inches for heat sink
3. Add regulators pg 3 U74 and U135 to raise supply voltage for analog switches in video chain to + -10V (U77, U78, U79, U86, U87, U88, U95, U96, U97, U104, U105, U108)
4. for each video channel move references (U132) close to ADC (U76) & decouple real close (C313) per doc from website. Application Note AN-931
5. Reference supply feed - move associated ground (to Gnd V) U123
6. Change decoupling cap size on video chain (U77, U78, U79)
7. Sprinkle in some large values caps - 50uF or so worth per chain on the +5.5V, -5V & +-10V
8. Move clock & bias test points behind output switches
9. Add test points on more serial lines (monitor DAC Writes, etc.) pg 1, U41 output pins Y2-Y9
10. Change filter caps on HV Bias input & feedback to 470pF c385, C373, C386, C374, C420, C403, C402, C419 for noise reduction input filter cap to 1uF (C48, C62, C50, C64, C423, C41, C39, C24)
11. Pg 6 change input filter caps bias from 0.01uF to 1uF C52, C66, C54, C68, C27, C43, C29, C45
12. take + - 10V to telemetry page 2 with resistors
13. Changed all 10uF tant 10V caps to 10uF 16V
14. U46 rearrange order of signals to be in order sw1-4 should be hvb4-8 in order like all other switches on the board
15. Pg 8 & 9 remove 0 ohm on ADC ref pin R251, r107, r125, R146
16. ADC 5.0 V reference chip input voltage now taken after inductors on +vana & -vana new power +VA_REF AND -VA_REF
17. Pg 4, 5 change all LT1358 op amps to LT1497, change feedback capacitor to be open all channels
18. Pg 10 add note to install JP1 & JP2 by default, show graphic that they are installed
20. Move TP58 closer to U107 for GND TP in this area

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21. Add test pt TP74 to GNDA locate it by U65, for GNDA test in power area
22. pg 1 U117 swap outputs lines, Chan2 now on 1B pins and Chan1 now on 2B pins, swap select lines accordingly for swapped outputs.
23. Change U128 to LT1175CS8 for part type consolidation add associated adjust resistors.
24. Pg 3 change grounds on C335, U65 pin 6,7 to GNDA
25. Change +VA_ref on U132, 128, 121 & 116 to +10V
26. remove JP1, JP2, on +-5V output to preamp and connect J2-17 to +10V and J2-20 to -10V, route on Layer 7 as copper from 10V source to connector, but isolated from other +-10V nodes within the channel.

This section to be completed by reviewing authority			
Review Date:		Reviewer(s):	
Disposition:	☐ Approved	☐ Denied	☐ Request Additional Information