NOAO

ENGINEERING CHANGE ORDER

BOARD NAME	TORRENT Local Control BRD LCB		ECO#	**TRNT-017**	DATE 19MAY11
BRD SERL#	ALL REV A	REV	ART#	TRNT-EL-07-0002-XXX	
PN#		REV			REV
ASBLY#	TRNT-EL-04-0002	REV A	PCB#	TRNT-EL-04-1002	REV A
BOM#	TRNT-EL-04-4002	REV A1	SCH#	TRNT-EL-04-2002	REV A
COGNIZANT ENGNR			APPROVD		

REASON FOR MODIFICATION:

1. Prevent power supplies VANA, VCB, VHV, VBB from turning on during initial fpga configure at power on.
This causes potential lethal voltages (for detectors) to appear on the detector output pins.

DRAWINGS AFFECTED:	NEW REV
TRNT-EL-04-0002	A1
TRNT-EL-04-2002	A1
TRNT-EL-04-4004	A2

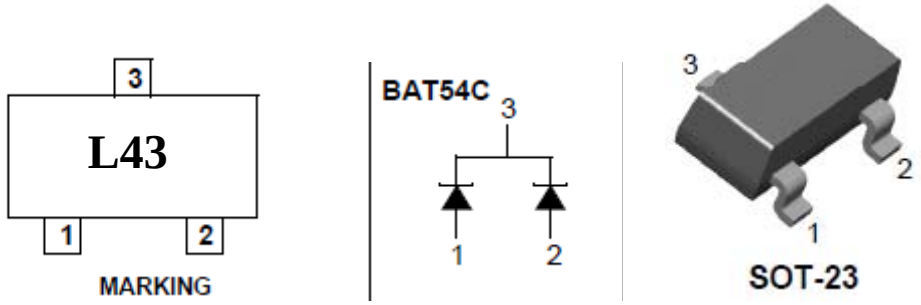
DESCRIPTION OF MODIFICATION:

1. Place diodes on U8:2 VCB_PWR_EN_OUT, U8:11 VANA_PWR_EN_OUT, and U8:15 VBB_ENBL_OUT.

- with anodes to U8 pins - and common cathodes tied together and connected to the DONE signal that can be found R64:2, TP5, U27:M15 & U43:13. See graphics for installation locations.

On bottom of board (opposite the Xilinx BGA)
See Figure 1 and 2, Figure 3 and 4 are additional information
Solder D2:2 to via highlighted in red, Solder D3:1 to via highlighted in red
Use white 30 or 32 awg wire, solder one end to red via by R107, the other end to lead of D2 (D2:1)
Use white 30 or 32 awg wire, connect D3:3 (K) to D2:3, connect D2:3 to TP5. Use RTV to tack long wire approximately where shown by the green X marks, avoid all pads & vias.
2. The following resistors are normally not installed: R68, R69, R108, R109

This section to be completed by reviewing authority			
Review Date:		Reviewer(s):	
Disposition:	☐ Approved	☐ Denied	☐ Request Additional Information


3
L43
1
2
MARKING
BAT54C
3
1
2
3
2
1
SOT-23

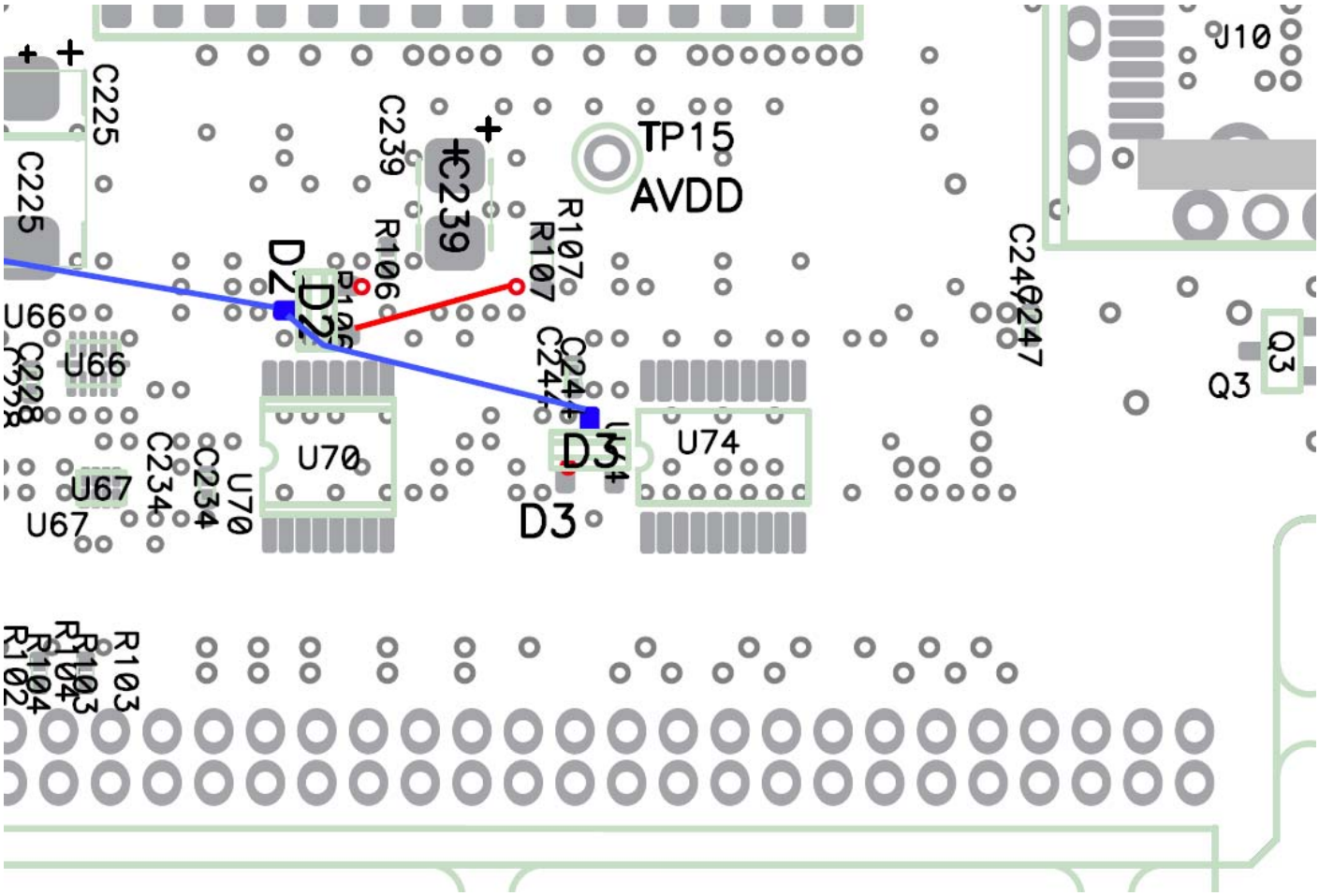

C225
C225
C239
C239
TP15
AVDD
R106
R107
R107
D2
U66
U66
U67
U67
U70
U70
C234
C234
D3
U74
J10
C247
Q3
Q3
R103
R104
R104
R102

Figure 1

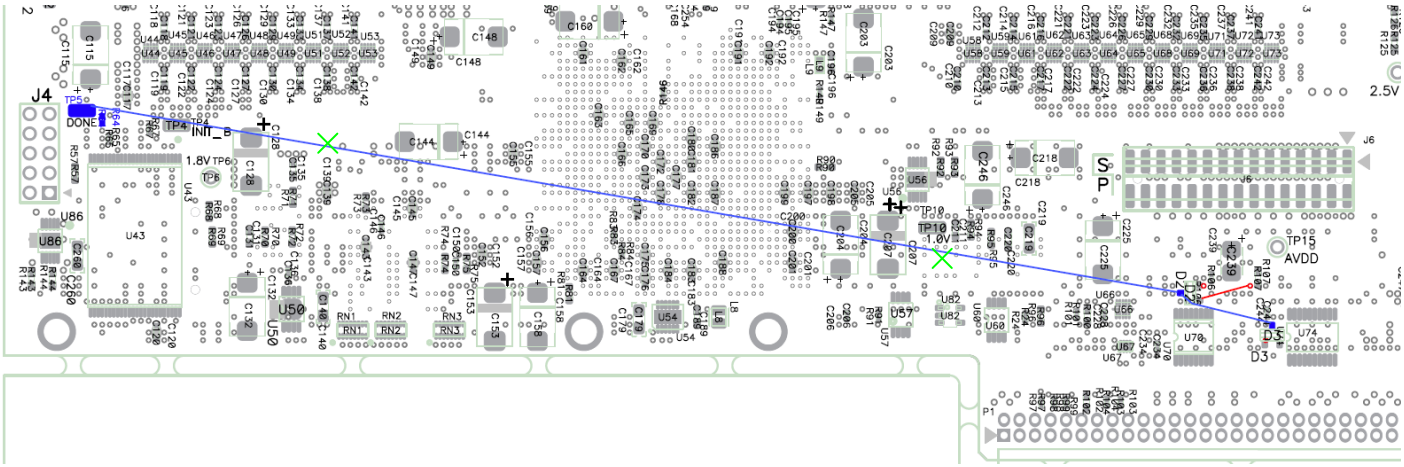


Figure 2

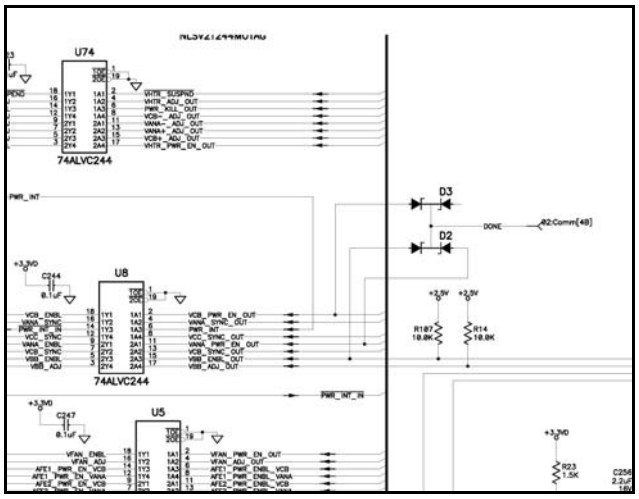


Figure 3
Schematic Pg 7

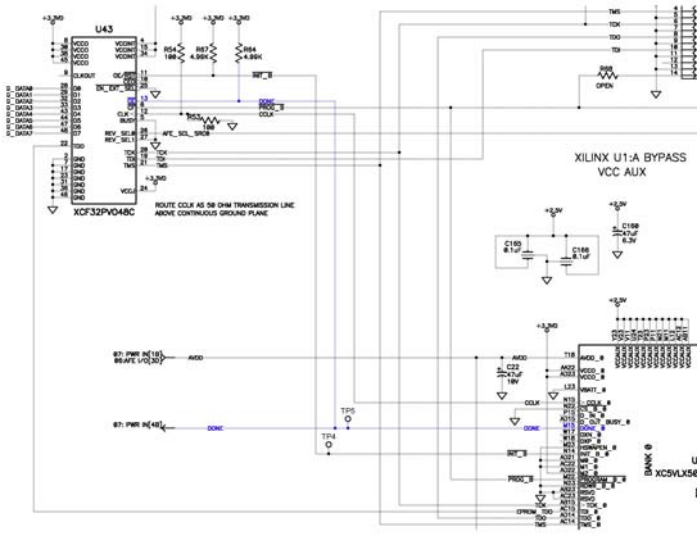


Figure 4
Schematic Pg 2

2. Remove resistors R68, R69, R108, R109

R68 - Enables the use of the 'boot after eeprom write' function of the JTAG interface
R69 Selects the clkout phase of U37
R108, R109 when installed, selects the backup firmware load on the GIGe interface