NOAO

ENGINEERING CHANGE ORDER

BOARD NAME	TORRENT Local Control Board (LCB)			ECO#	**TRNT-012**	DATE	9/15/2010
BRD SERL#	Starting at 005	REV		ART#			
PN#		REV				REV	
ASBLY#	TRNT-EL-04-0002	REV	OD	PCB#	TRNT-EL-04-1002	REV	OD
BOM#	TRNT-EL-04-4002	REV	OD	SCH#	TRNT-EL-04-2002	REV	OD
COGNIZANT ENGNR				APPROVD			

REASON FOR MODIFICATION:

Functional corrections to physical and electrictric elements

DRAWINGS AFFECTED:	NEW REV
TRNT-EL-04-0002	A
TRNT-EL-04-1002	A
TRNT-EL-04-2002	A
TRNT-EL-04-3002	A
TRNT-EL-04-4002	A

DESCRIPTION OF MODIFICATION:

Item	Originator	Action Description	Status
1	dms	fix item #74 on bom to correct PN 16 term CTS	
2	dms	replace vias with direct connect vias - at least correct thermals	
3	dms	bga and lga parts all vias under should be barrel relieved.	
4	dms	fix L10 on layout to correct component outline please provide complete PN	
5	dms	add a ground strap to the board and/or loop test points	
6	dms	replace U31, with new library element to reflect correct size of part, move R52 away from the U31	
7	dms	make sure gerber pad data is solid pads	
8	dms	look at reducing the pad size on all NLSX3014 parts to allow some mask between lands. Make resist tight on sides of pad but leave room for fillets on the ends.	
9	dms	review camtek email on 3/30/09 (7) issues with gerber	
10	dms	PL #23 add C239 in refdes column	complete
11	dms	shield connection on J8, J9, j10	
12	dms	Fiducial near U37 clear top layer copper pour away more	complete
13	dms	C148 move "+" to better location	complete
14	dms	J4 needs pin 1 marking on SS	
15	dms	U80 pin 1 marking move off via	complete
16	dms	c117 skewed part fix thermal imbalance	complete

17	dms	Part list add 2 rohs labels, note on assembly locations and labels added post cleaning process.	
18	dms	Parts list add blank PCB	
19	dms	fab print rohs label area prohibit vendor markings	
20	dms	R13 line it up components above it	
21	dms	selection of I2C serial number part	complete
22	dms	add I2C serial number IC & connections (addressing issue) LCB EEprom U25 4 (1,2,7 = gnd)(3 = 3.3V) fix LCB TS1 U26 1 (5,6 = gnd)(7 = 3.3V) okay LCB TS2 U57 2 (5,6, 7 = gnd) okay LCB SSN N/A N/A N/A N/A	need to
23	pcm	Change SPT connector for fixed transceiver - if the GIGe product wors. This would prevent accidental extraction of transceiver when trying to remove fibers.	revisit
24		replace lib element LTM4608 (U37&U20) in schematic, this should disconnect 4C & 5C from the SVIN net. Remove traces from 4C & 5C	
25		change fan connector to right angle and move toward tab so that it will fit.	
26	dgs/dms	swap sides of board reset sw & fan con	
27	dgs/dms	review lt3080 package options to MS or DD	
28	pcm	P4, add pins for digital ground.	
29	dgs/pcm	Reverse connections to FPGA pins G1 and H1. G1 should be SPF_RD+ and H1 should be SPF_RD-.	
30	pcm	Add a low pass filter to pin 32 (CP) of LMK03000 clock conditioner. I've worked out some values for the three components that we need to put on the CP node (pin 32) of the LMK03000 device (U28) on the LCB board. Please update the redline for the LCB and if possible, try to kludge these on the LCB prototype board in Tucson for test. 1. From pin 32 on U28 connect a ceramic 5% 5.6nf 25v NPO capacitor to ground. 2. From pin 32 on U28 connect a ceramic 5% 7.5nf 25v NPO capacitor via a 1% 3.60K series resistor to ground.	
31	pcm	Seriously look at supplying a separate and localized 2.5v supply to the GIGe device close to the flex connector. As it is the supply to the GIGe is @ 2.42volts due to the voltage drop across the pcb lands from U9. In addition, this would better isolate the GIGe digital noise from the LCB logic.	
32	pcm	Remove R66 and connect u27 PIN n22 (/CS_B_0) to gnd	
33	pcm	Consider replacing the SFP modular Fiberxon FTM-8120C-LG transceiver with a board mount version Intel TXN310110000000	
34	all	silk screen slot label "AFE1" & "AFE2" by the correct connectors rename all "AFE1_...." to "AFE2_..." and "AFE0_..." to "AFE1_..."	
35	all	before editing net names send off a was/is list for approval. In the I2C area	
36	pcm 6/25/09	1. Remove signal I2C_SNS_EN from U22 pin 12. Connect pin 12 U22 to pin 1 U22 (VL).	

37	pcm 6/25/09	2. Remove signal I2C_SRC_EN from U23 pin 4. Connect the signal I2C_SNS_EN from step one to U23 pin 4. Rename the signal I2C_SNS_EN as I2C_SDA_EN.
38	pcm 6/25/09	3. Swap signals from the inputs and outputs of U23 pin 2 (input) and 7 (output) with U24 pin 2 and 7.
39	pcm 6/25/09 & 07/06/09	4. Remove signal I2C_SRC_EN from U66 pin 12. Connect pin 12 U66 to pin 1 U66 (VL) +2.5V.
40	pcm 6/25/09	5. Remove signal I2C_SRC_EN from U67 pin 4. Connect the newly named signal I2C_SDA_EN from step 2 to U67 pin 4.
41	pcm 6/25/09	6. Swap signals from the inputs and outputs of U67 pin 2 (input) and 7 (output) with U14 pin 2 and 7.
42	pcm 6/25/09	7. Rename the signal I2C_SRC_EN to be I2C_SCL_EN.
43	pcm 7/9/09	1. Disconnect signal LCB_RESET from pin 9 (/1A) of U70 leaving the pullup (R18) connected to the FET drain (Q3).
44	pcm 7/9/09	2. Disconnect signal /REBOOT from pin 11 (/R) of U70 and reconnect to pin 9 (/1A) of U70 leaving the resistor and capacitor (R105 & C231) connected to pin 11.
45	dms 7/24/09	relocate ground vias under C239 to reduce potential shorts.
		LVPECL Clock Termination fix:(following 4 items)
46	pcm 7/27/09	1. Remove series resistors R29, R30, R33, R34, R35, R36 from nets /TCLK, TCLK, /MCLK, MCLK, /PCLK, PCLK.
47	pcm 7/27/09	2. Add shunt 180 Ohm resistors on the above nets to GND.
48	pcm 7/27/09	3. Change the value of the termination resistors R31, R37, R82 to be 100 Ohms.
49	pcm 7/27/09	4. Add shunt resistors and termination resistors to clock net DCLK.
50	dms 7/27/09	TSM_PRESENT, ~TSM_PRESENT (J13) what is the permanent solution
51	dms 7/27/09	R24 - move to bottom of the board so that part will solder to the board.
		Correction OCLK PECL Termination: (following 2 items)
52	pcm 7/27/09	1. Add a 180 Ohm shunt resistor from FPGA pins J14, H13 (OCLK, /OCLK) to GND
53	pcm 7/27/09	2. Add a 100 Ohm termination resistor between these signals and as close as possible to the FPGA pins.
54	pcm 8/10/09	1. Remove GND connection from the memory device U31:A balls F3 and B3
55	pcm 8/10/09	2. Connect U31:A ball F3 to signal LDM (ball V25 on FPGA - U27:F)
56	pcm 8/10/09	3. Connect U31:A ball B3 to signal UDM (ball W29 on FPGA - U27:F)
57	pcm 8/19mtg	move J4 up about .2 inches and add a 9th pin that goes to ground.
58	dms 8/26/09	LS2 connector, graphic depicting orientation of socket /pin in silkscreen

	dms	make sure all LFN, DFN package parts have enough pad
59	6/09/10	(LTC2801CDE#PBF & NLSX3014MUTAG)