NOAO

ENGINEERING CHANGE ORDER

BOARD NAME	TORRENT CCD AFE BOARD			ECO#	**TRNT-007**	DATE	1/4/2010
BRD SERL#	006 >			ART#			
PN#		REV				REV	
ASBLY#	TRNT-EL-04-0004	REV	OD	PCB#	TRNT-EL-04-1004	REV	OD
BOM#		REV		SCH#	TRNT-EL-04-2004	REV	OD
COGNIZANT ENGNR				APPROVD	Mark Hunten		

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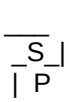
Date: 2010.05.20 11:48:19 -07'00'

REASON FOR MODIFICATION:
Get board functioning

DRAWINGS AFFECTED:	NEW REV
TRNT-EL-04-0004	A
TRNT-EL-04-1004	A
TRNT-EL-04-2004	A
TRNT-EL-04-3004	A
TRNT-EL-04-4004	A

DESCRIPTION OF MODIFICATION:

Item	Originator	Action Description	COMMENTS
1	pcm 07/07/09	for R62 (the resistor between the AFE_SDA_SRC and AFE_SDA_SNS signals on page 11). The resistor value should change from 2.0K to 825 Ohms.	
2	dms 07/20/09	change U140 from TSSOP to SOIC that was ordered for all boards	
3	DMS 07/29/09	mount JT1 on bottom of board opposite silk screen, correct layout if respin. To make accessible from visible side of board.	
4	dms 08/13/09	fix land pattern for DGG parts SN74ALVC16834DGGR,	
5	dms 08/13/09	fix land pattern for AQV252GA	
6	dms 08/13/09	check DGV patterns since they did not wet properly	?
7	dms 8/19/09	change from ENIG to lead free HASL	none issue stay with ENIG
8	dms 8/19/09	review assembled board, look for interferences and proximity problems.	
9	dms 8/26/09	LS2 connector, graphic depicting orientation of socket /pin in silkscreen 	
10	dms 9/14/09	swap of clocks 2 & 3 at U8, causes inconsistence at J1, next cut reorganize so that J1 is consistent, even clks on even pins odd clks on odd pins	
11	9/16/09 group	Does +-5VRTn influence channel 1, if yes, decide what should be .	unable to evaluate at this time
12	mh 9/21/09	R85 and R86 values reversed. Move R85 1.0K to connect between pin 2 and ground, move R86, 3.09K, to be connected across pin 1 and pin 2	

13	dgs 9/21/09	PG 7, U46 and U53 should be connected to +-VAHI rails (not +-VALO rails)	
14	dgs/pcm 9/21/09	All MAX312 parts (16 items) have the input and switch enable pins reversed	repair library element
15	dgs/pcm 9/21/09	Add protection diodes to the VP and VN supplies at the power/data connector. VP80, VP180, and VP300 should have the cathode toward the positive supply. The VN80, VN180, and VN300 supplies should have the cathode toward ground. ZHCS500TA	redundant protections so long as space allows.
16	dgs/pcm 9/21/09	The connections to the inverting and non-inverting pins of U130, U124, U119, and U114 are reversed. Pins 3 & 6 of the switch should go to the non-inverting input (pin 3) of the op amp and pins 11 & 14 of the switch should be connected to the inverting (pin 2) input.	
17	dgs 9/22/09	Pull up resistors are needed on all of the AD7982 SDO data outputs. Add TBD ohm resistors between 3.3V and each of the ADC_DATA0 thru ADC_DATA3 nets.	added to Pg 1, U100
18	pcm 09/22/09	The disable (pin 7) of the ADA4941 devices (U75, U84, U93, U103) should be tied to -5V instead of GND.	
20	dgs 10/5/09	AFE_DATA_EN needs to be /AFE_DATA_EN	
21	pcm 10/07/09 TRNT meeting	U140 24AA128 eeprom Pin 7 (WP) should be tied to ground	
22	dgs 10/8/09	U145 should be wired as a voltage follower (copy of U134), i.e. gain=1, to preserve the 0-5V telemetry voltage range from the MUX to the ADC.	(use graphic on eco) see figure 1
23	dgs 10/30/09	/TELADC0_DOUT CHANGE TO TELADC0_DOUT	
24	dgs 11/2/09	The clock state switches (e.g. U28 for clock 0) are shown in the logic "1" state. Thus, the clock low state is wired to the logic high input. Should this be rewired for all clock channels? Currently this is corrected in firmware. Additionally logic state 0 should be VCLKLO signal, requires signals on pins 6 & 4 to be swapped.	change sch symbol to be drawn in the logic 0 state, additionally logic state 0 should be VCLKLO signal, requires signals on pins 6 & 4 to be swapped & rerouted.
25	dgs 11/04/09	U64 latch has the test point signals scrambled. This either requires re-routing the signals (see Dave's marked up schematic) on the input or output of the latch and the LOAD signals. Or the registers can be scrambled in firmware to correct for the mapping order.	used reroute option
26	dgs/dms 11/05/09	Should the MAX312 switches in the test point circuit be changed to the NO version? This would prevent the test signals from being shorted if the part is not energized. Also, might be power saving because only one channel (instead of 3) would need to be energized to select TP signal.	change all MAX312L parts on Pg 10 to MAX313L
27	dms 1/8/10	change test points to trapezoid style	
28	dgs/mh 1/11/2010	move 2.0K R250 et al to the output side of the switch.	
29		U66 (S12) to gnd (red line on the sch)	
30		AFE_CTRL_ENABLE change to ~AFE_CTRL_ENABLE (red line on the sch)	wrong, comments from Peter change this back to "high true"

31	as per ICD	AFE EEprom U140 (1,2,7 = gnd)(3 = VPIFC) AFE TS1 U151 (5,6, 7 = gnd) AFE TS2 U70 (5,6 = gnd)(7 = VPIFC) AFE SSN U72 0 hard wired into device	
32	dms	add cap on comp pin of ad829 to -5v as option	
33	mhunten	U79, U88, U97, U108, ADG701 change to MAX4648, from single supply to dual supply type.	
34	rgeorge, mhunten	compensation cap value change, C315, C283, C226, C247 from 15pF to 68pF	
35	dgs/pcm3/15/10	R63, R68, R99, R117, R135, R152, R157, and R178 to change to 75 Ohms and R151 to 0 Ohms	
36	4/14/10 torrent meetg	Normalize voltage input names AFE_VP80A = VANA+ AFE_VN80A = VANA- AFE_VP180A = VCB+ AFE_VN180A = VCB- AFE_VP300A = VHV+ AFE_VN300A = VHV-	
37	pcm cmnts in rA-PR-1revised pcm sch	R80, R81, R259, R260, R261 changed to 10K, R262 change 3.32K to conserve power and bring all "normal" values to half scale on ADC Output.	
38	pcm cmnts in rA-PR-1revised pcm sch	remove out of date notes & comments from schematic	
39	pcm cmnts in rA-PR-1revised pcm sch	all x2y capacitor types on page 3 can be changed to regular cerc type caps	
40	pcm cmnts in rA-PR-1revised pcm sch	FB1 & FB4 parts change to DR74-221-R inductors, since they are on the other supplies.	
41	rvw w/MH 5/13/10	check distribution and type, value of bypass caps for U18,U19, U32, U33, U20, u22, u34, u35, circuits are dis-similar	
42	pcm cmnts in rA-PR-1revised pcm sch	remove 10 ohm resistors on power rails U83 et all all channels.	
43	rvw w/MH 5/13/10	change MAX312L TO MAX313LESE+ U77 & U78 location all channels	
44	pcm cmnts in rA-PR-1revised pcm sch	R103, R104 location to be matched 1K pair all channels	
45	pcm cmnts in rA-PR-1revised pcm sch	R97 0 ohm all channels	
46	pcm cmnts in rA-PR-1revised pcm	U132 pin 3 to 1uF cap to ground, all channels	

47	PCM comments & jrg 3/14/10	Pg 3 U74, disconnect pin 5 from ground, pin 4 from pin 6 node, leave pin 5 open and connect pin 4 to ground, pin 6 remains connected to R87. R83 change value to 2.21K, R84 change value to 1.5K	
48	Pcm/mh	At J2 break + & - 5V connection with a jumper to allow different power to be sent to the transition board	

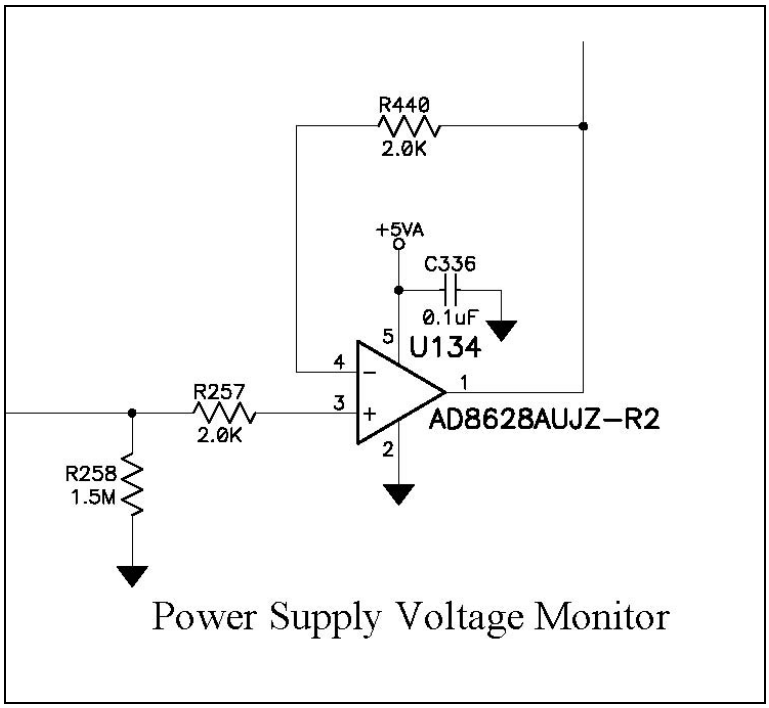


Figure 1
Item 22 on action list