



SL100/SL240
Hardware Reference
for PCI, PMC, and CPCI Cards

Document No. F-T-MR-S2PCIPMC-A-0-A6

FOREWORD

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FCC

This product is intended for use in industrial, laboratory or military environments. This product uses and emits electromagnetic radiation, which may interfere with other radio and communication devices. The user may be in violation of FCC regulations if this device is used in other than the intended market environments.

CE

As a component part of another system, this product has no intrinsic function and is therefore not subject to the European Union CE EMC directive 89/336/EEC.

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1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

This manual introduces the FibreXtreme SL100/SL240 family of products to users, and guides them through the process of unpacking, setting up, and programming the cards.



NOTE: Both the FibreXtreme SL100 and SL240 hardware are referred to throughout this manual as SL240. The software that supports both the SL100 and SL240 hardware is referred to as SL240, including the driver and API. Anything that is exclusive to the SL100 or the SL240 is described as such.

1.1.2 Scope

This manual contains the following information:

- An introduction to FibreXtreme SL240.
- Applications and topologies for SL240 boards.
- Instructions for installing and configuring the board.
- An operational overview of the product.
- General board specifications.
- Register set information.
- Programming information.
- Summary of the protocol used by the SL240 boards.
- Ordering information for all products mentioned in this manual.
- A brief introduction to the Front Panel Data Port (FPDP) interface.
- Definitions of words, phrases, and terms used in this manual.
- List of key words referenced in this manual.

The information in this manual is intended for information systems personnel, system coordinators, or highly skilled network users with at least a systems-level understanding of general computer processing, memory, and hardware operation.

1.1.3 Style Conventions

- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a “0x” prefix. For example, 0x7e.
- For signals on hardware products, an ‘Active Low’ is represented by prefixing the signal name with a slash (/). For example, /SYNC.

- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

C:\>ls		
file1	file2	file3

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- *ANSI Z136.2-1988 American National Standard for the Safe Use of Optical Fiber Communication Systems Using Laser Diode and LED Sources.*
- *Draft Standard for a Common Mezzanine Card Family: CMC; IEEE P1386, Draft 2.0, April 4, 1995.*
- *Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC, IEEE P1386.1, Draft 2.0, April 4, 1995.*
- *Fibre Channel Association Product Information Bulletin Revision, December 9, 1994.*
- *Fibre Channel Physical and Signaling Interface (FC-PH), Revision 4.3, June 1, 1994; Produced by the ANSI X3T9.3 standards group.*
- *Fibre Channel Physical and Signaling Interface-2 (FC-PH-2), Revision 7.3, January 5, 1996; Produced by the ANSI X3T11 standards group.*
- *Fibre Channel Physical and Signaling Interface-3 (FC-PH-3), Revision 8.6, April, 1996; Produced by the ANSI X3T11 standards group.*
- *Front Panel Data Port Specifications, ANSI/VITA 17-1998, Revision 1.0; February 11, 1999. Produced by the VITA Standards Organization.*
- *IEC 825-1984 Radiation Safety of Laser Products, Equipment Classification, Requirements, and User's Guide, 2 parts, 1993.*
- *LinkXchange LX1500e Crossbar Switch Hardware Reference Manual (Doc. No. F-T-MR-LX1500E), Systran Corp.*
- *LinkXchange LX2500 Crossbar Switch Hardware Reference Manual (Doc. No. F-T-MR-LX2500), Systran Corp.*
- *PCI Local Bus Specification, Revision 2.1, June 1, 1995; PCI Special Interest Group.*
- *CompactPCI Specification, Revision 3.0, October 1, 1999; PICMG 2.0; CompactPCI Power Interface Specification, Revision 1.0, October 1, 1999; PICMG 2.11; Keying of CompactPCI Boards and Backplanes, Revision 1.0, October 1, 1999; PICMG 2.10.*
- Fibre Channel Association - <http://www.fibrechannel.com/>.
- Systran Corp. - <http://www.systran.com/>.
- VITA - <http://www.vita.com/>.

1.3 Quality Assurance

Systran Corporate policy is to provide our customers with the highest quality products and services. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. Our quality commitment begins with product concept, and continues after receipt of the purchased product.

Systran's Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production,

installation and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

- Achieve, maintain and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Systran's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Systran's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

Customer feedback is integral to our quality and reliability program. We encourage customers to contact us with questions, suggestions, or comments regarding any of our products or services. We guarantee professional and quick responses to your questions, comments, or problems.

1.4 Technical Support

Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

If you have any technical or non-technical questions or comments, contact us. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: **(937) 252-5601** or **(800) 252-5601**
- E-mail: **support@systran.com**
- Fax: **(937) 252-1349**
- World Wide Web address: www.systran.com

1.5 Ordering Process

To learn more about Systran products or to place an order, please use the following contact information. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: **(937) 252-5601** or **(800) 252-5601**
- E-mail: **info@systran.com**
- World Wide Web address: www.systran.com

2. PRODUCT OVERVIEW

2.1 Overview

The FibreXtreme SL240 cards provide fast, low latency point-to-point or broadcast connections between sensors and processing devices. Systran's SL240 family of products includes PCI, PCI Mezzanine (PMC), CompactPCI (CPCI) and Front Panel Data Port (FPDP) solutions. The FPDP versions are split into two categories—a 6U VME based solution with standard FPDP connectors and a rehostable Common Mezzanine Card (CMC).

The PCI, PMC, and CPCI versions provide this link via the PCI bus. The PCI bus is used in most standard PCs, and the PMC format is used in most popular single-board computers. CompactPCI is a 3U or 6U Euro card format PCI card designed as a more mechanically robust alternative to desktop PCI cards. The FPDP versions of the card provide this interface through a simple unidirectional parallel port. This port can be connected to existing FPDP equipment (VME) or can be integrated into new products (CMC). All of these variations interoperate completely on the link interface, providing seamless integration between diverse platforms.

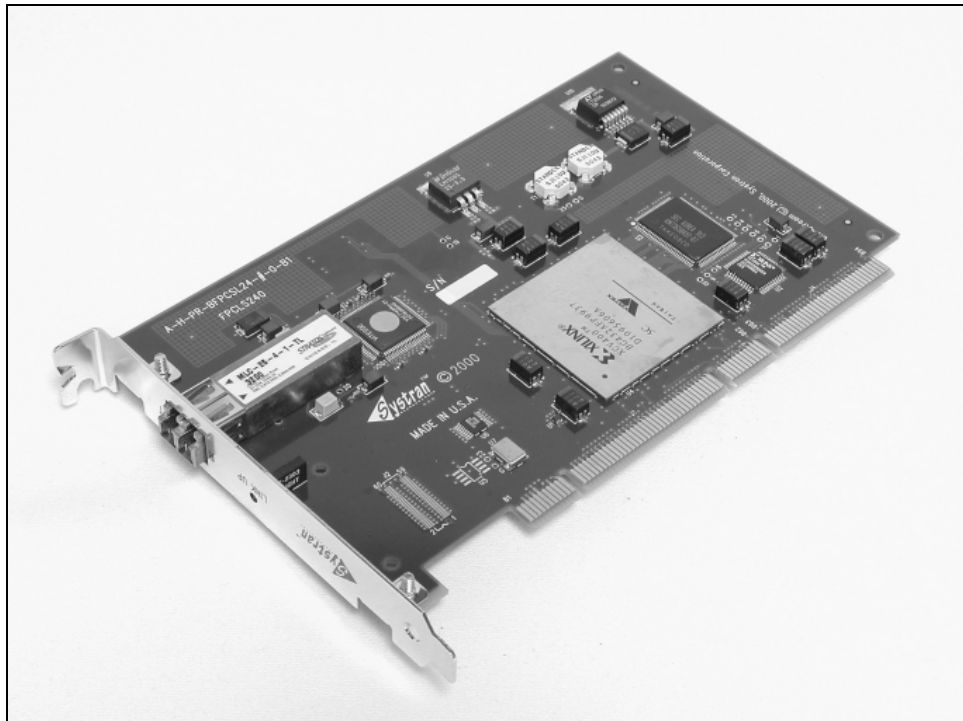
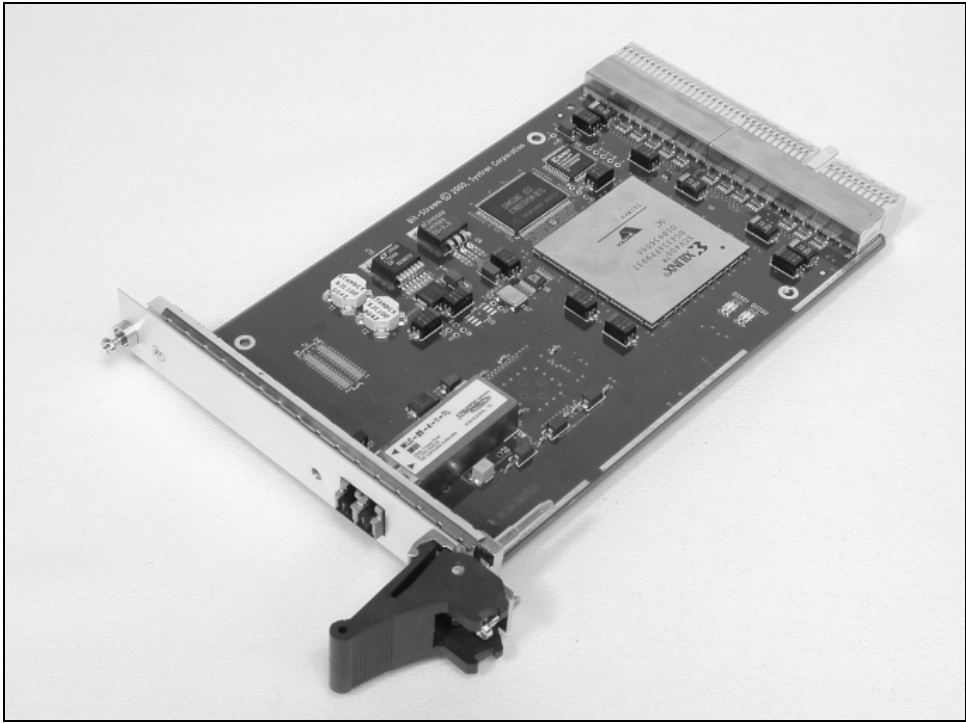
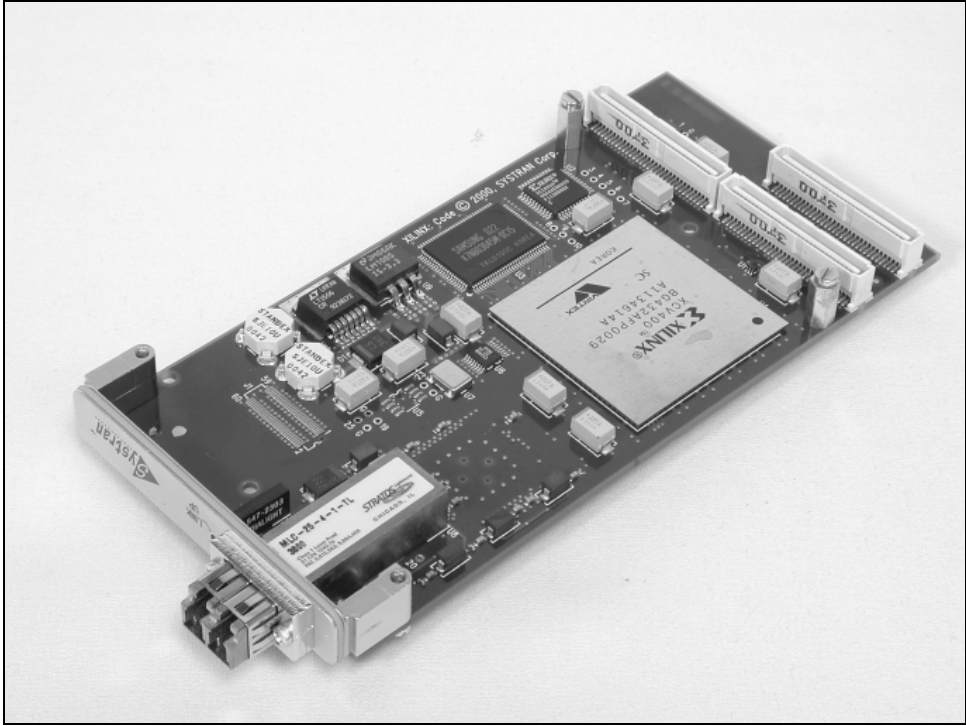


Figure 2-1 SL240 PCI Board



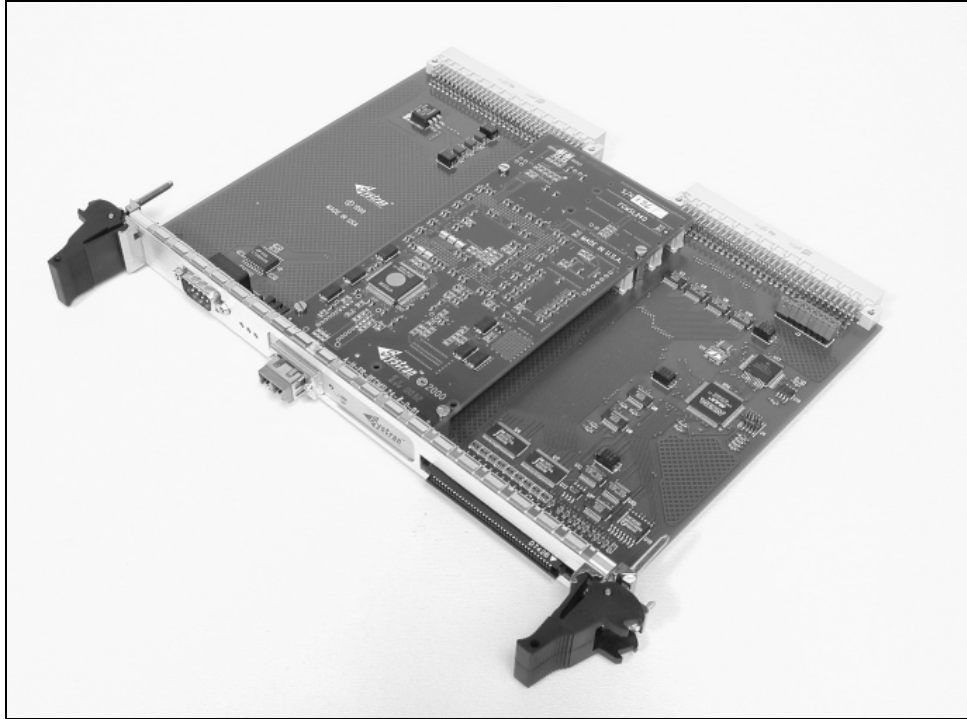


Figure 2-4 VME Adapter with CMC Board

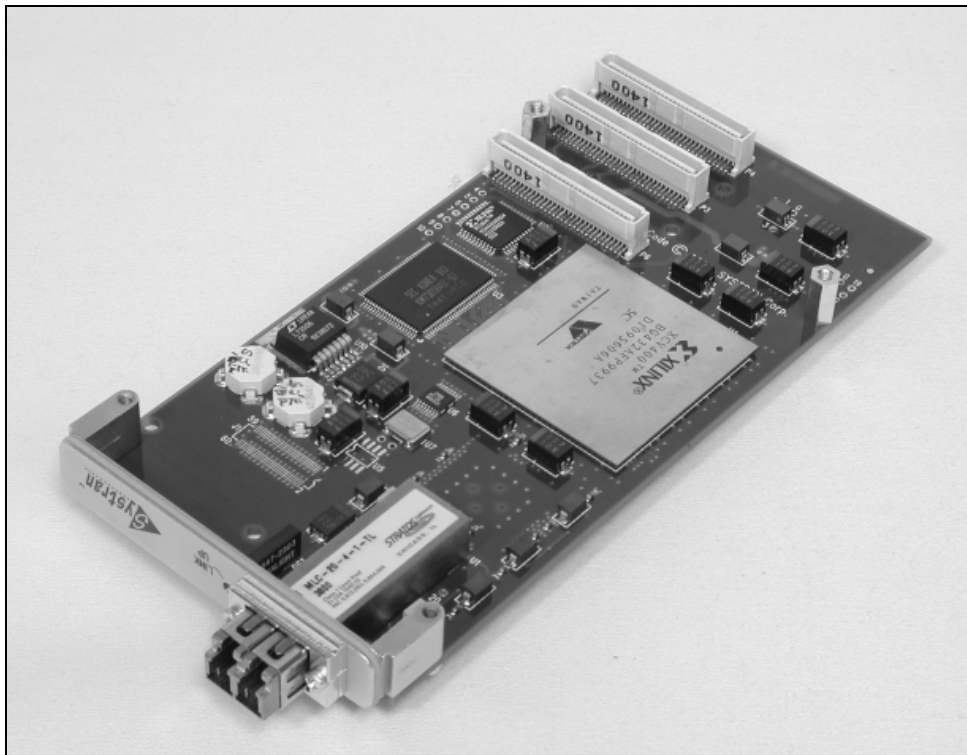


Figure 2-5 CMC Board

2.2 SL240 Features

SL240 provides reliable point-to-point or broadcast interconnects between systems, with minimal overhead and very low latency. The protocol involved for this transport is based on Fibre Channel, though it is not Fibre Channel compliant. The major SL240 features are listed below:

- Uses proven 8B/10B encoding for data transmission.
- End-to-end throughput of 247 MB/s with or without frame checksums (SL240).
- End-to-end throughput of 105 MB/s with or without frame checksums (SL100).
- Minimizes implementation cost and enhances throughput by using a simple protocol.
- Provides built-in data synchronization with very little reduction in throughput.
- Integrated interrupt controller to report link failure, transaction completion, or buffer space request.
- Status LED that reports link stability.
- Loop operation with out-of-band arbitration or point-to-point operation.
- Provides a register set designed for easy programming and status retrieval.
- Three media options available—long wavelength, short wavelength laser, and HSSDC copper.
- Watchdog timer for failover operation.
- 64-bit operation is backward compatible to 32-bit, 33 MHz.
- 1 MB Receive FIFO.
- 4 KB Transmit FIFO.
- Rugged versions of some cards available.

2.2.1 Media Options

There are three basic media options—a long wavelength laser (1300 nm) and short wavelength laser (850 nm), and HSSDC copper. Long wavelength laser interconnections are recommended for distances longer than 300 m, as loss in multimode fiber degrades connections with short wavelength lasers past this distance. HSSDC interconnections are recommended for very short distances of 30 meters or less.

The short wavelength version is useful for intrasystem connections, where you are connecting between cards on the same backplane. It is also suited for short reach intersystem connections (< 300 m).

All cards use a Duplex LC style connector or HSSDC receptacle, available from most major cable manufacturers. For details concerning these connectors, contact Systran Technical Support.

2.3 Applications

SL240 cards are used in a variety of topologies for a variety of applications. The following sections detail typical topologies used and some applications. Many other applications are possible in these configurations.

2.3.1 LinkXchange LX2500 Crossbar Switch (LX2500)

Systran's LX2500 Crossbar Switch provides the following features:

- Up to 32 non-blocking media-specific I/O ports.
- Up to 2.5 Gbps/port baud rate (port card dependent).

- Support for multiple point-to-point, loop, and broadcast communication links simultaneously.
- Automatic I/O Port fault isolation.
- Multiple media options.
- Out-of-band control through an RS-232 port.
- Can be connected to a modem and controlled from a remote location.

For more detailed information regarding LX2500 features and operation, contact Systran and request a copy of the *LinkXchange LX2500 Crossbar Switch Hardware Reference Manual* or visit our web site.

2.3.2 Typical Digital Signal Processing (DSP) Imaging System

With the support for 1.0625 Gbps or 2.5 Gbps link transmission rates between interconnected subsystems, SL240 is ideal for use in many of today's high-throughput data transfer applications. One example is shown in Figure 2-6. This figure shows the SL100's usable data throughput rate. However, the figure is also applicable to SL240 by changing the data throughput rate to 247 MB/s.

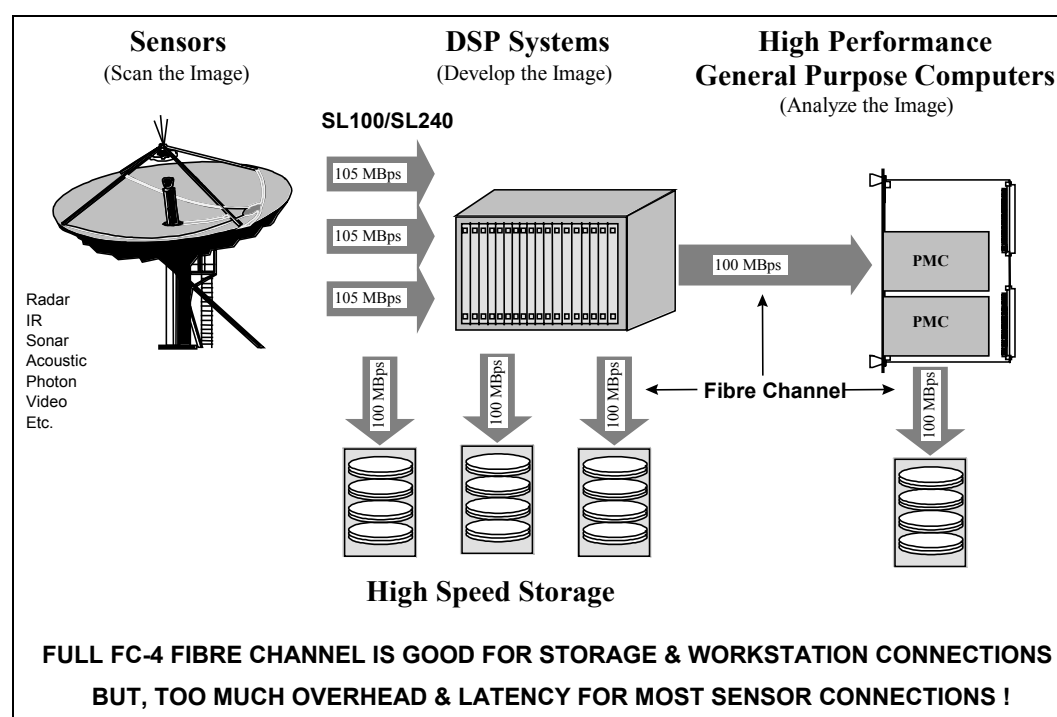


Figure 2-6 Typical Applications of FibreXtreme SL240 in Advanced DSP Systems

2.3.3 Extending FPDP

The maximum allowable length for FPDP cables ranges from 1 m to 5 m depending upon its configuration. The FibreXtreme SL240 system provides a communication link that extends the reach of FPDP while retaining simplicity, high bandwidth, and reliability. The type of laser transceiver used determines the distance the FPDP cards can be separated. See section 2.2.1, Media Options, for details on laser transceivers. It also provides a means of electrical isolation using fiber optics. This concept is shown in Figure 2-7.

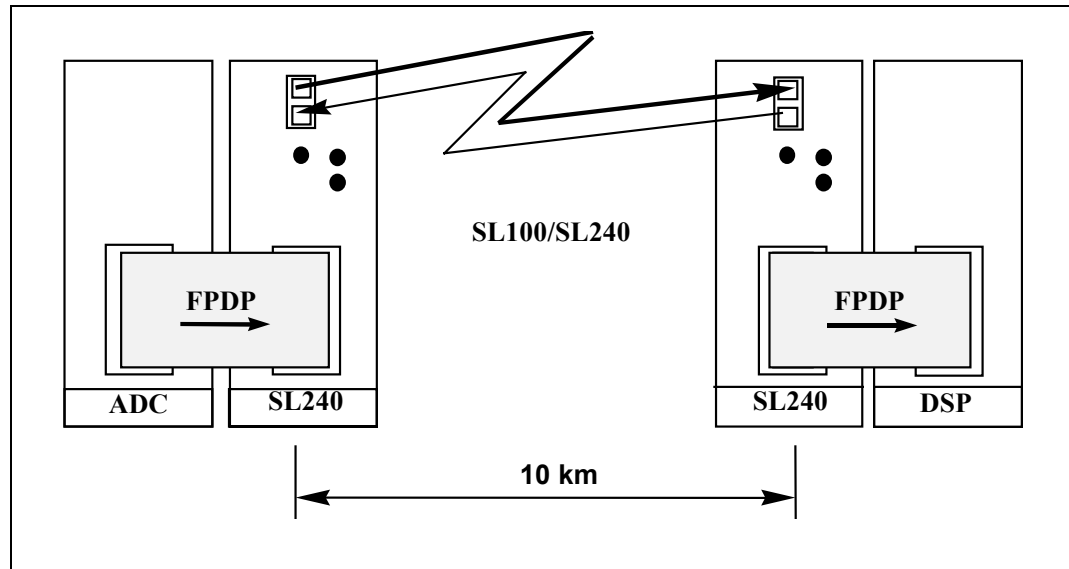


Figure 2-7 FibreXtreme SL240 Extending FPDP

2.4 Topologies

2.4.1 Typical Topologies

There are four typical topologies for the SL240 card. These topologies should cover most customer applications, though if another topology is desired contact Systran Technical Support to see if it is possible. The topologies are:

- Point-to-point
- Chained
- Single Master Loop
- Multiple Master Loop

2.4.2 Point-to-point

The point-to-point topology is the native mode for the SL240 card. One user option available in this mode is whether flow control is used or not. If flow control is used, the transmitter on each end will not transmit when the remote receiver is telling it to back off or the receive fiber is missing. In this mode, the maximum amount of data that can be transferred is 247 MB/s per direction (in this case, both cards are receiving and transmitting 247 MB/s at the same time). The maximum distance between the nodes is 10 km.

There are many applications for the point-to-point topology—as long as it involves only two nodes, this topology covers it. One advantage that point-to-point has over the other topologies is the ability to do simultaneous bi-directional traffic.

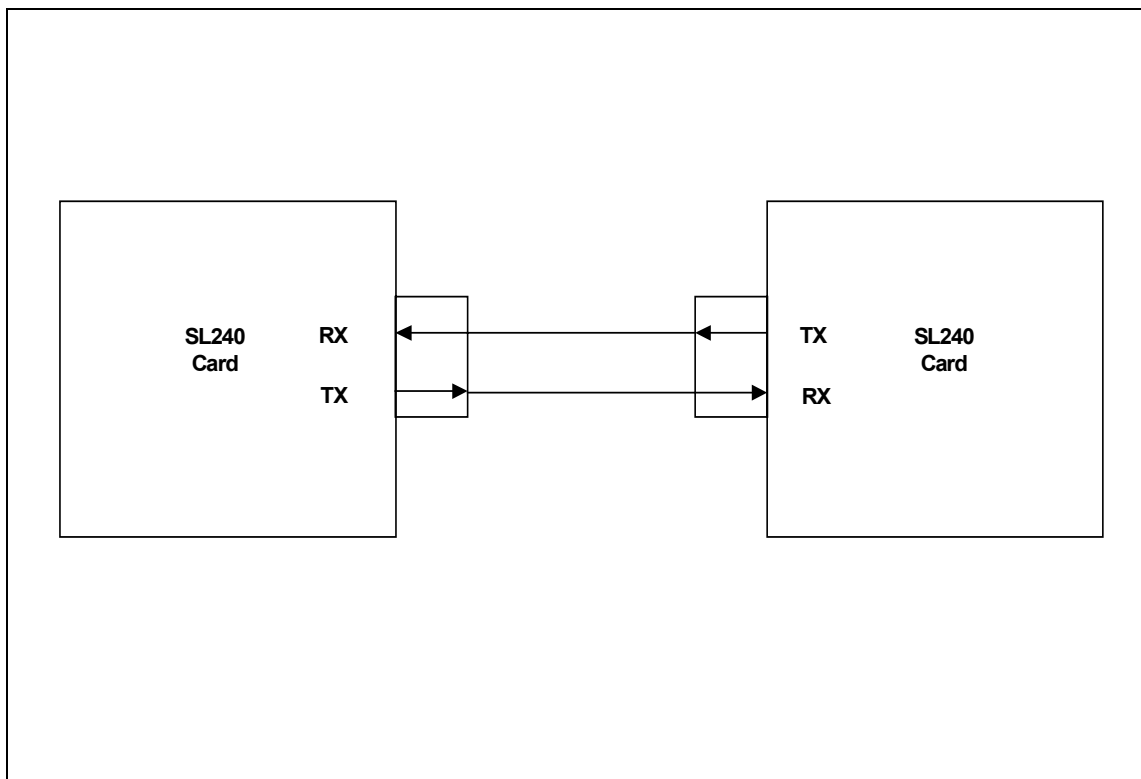


Figure 2-8 Point-to-Point Topology

2.4.3 Chained

This topology is a single transmitter on the end of a long string of receivers. No flow control is available in this topology, and the distance between the nodes is limited only by the transceivers used (10 km typical).

This topology is good for broadcasting data to multiple destinations where late data is of no use, such as video transmission applications.

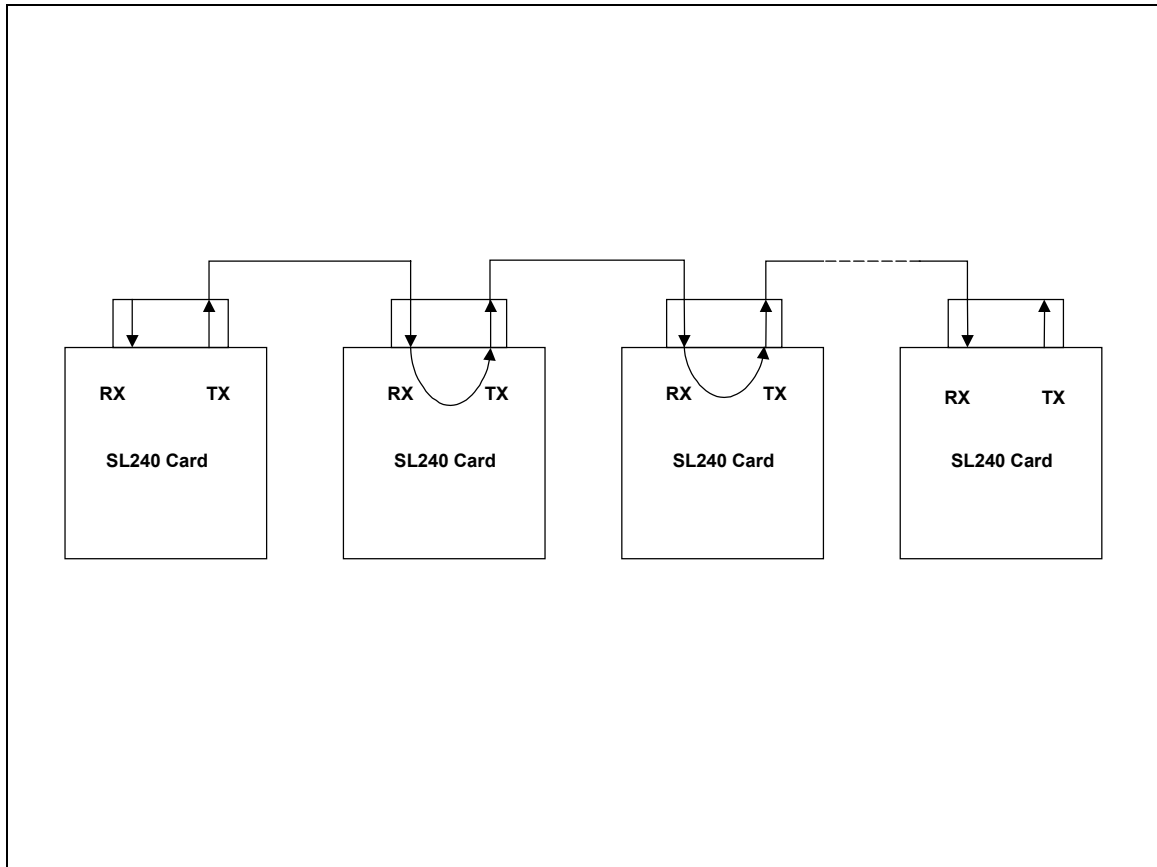


Figure 2-9 Chained Topology

2.4.4 Single Master Ring

This is one of the most useful topologies for the SL240 card. This topology allows a single transmitter to send data to a group of destinations with flow control from all of the destinations. This flow control is a single flag to the master—it can send or it cannot send data. This means that if one destination has a failure and stops removing data from its receive FIFO, it should be switched out to avoid bringing down the loop. A switch suitable for this purpose, the LinkXchange LX2500 Crossbar Switch, is available from Systran. Software controls mastership switching of the ring. There are rules associated with master switching listed in the “Programming Interface” section. The flow control used in this case is similar to a multi-drop FPDP bus, where any receiver can back the transmitter off.

This is the typical configuration for record-playback systems, where you have multiple signal processors and data storage elements present on the network and there is only one (the data source or the recorder playing the data back) transmitting at a time.

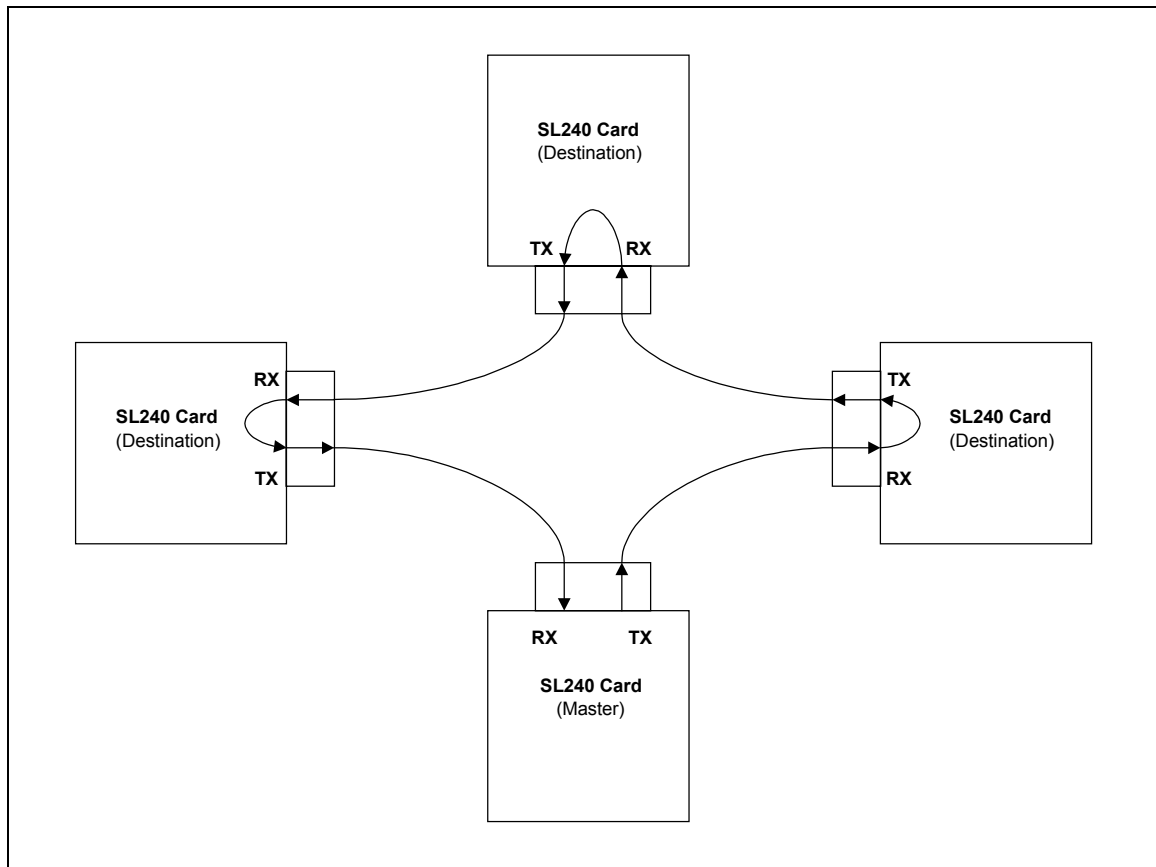


Figure 2-10 Single Master Ring

2.4.5 Multiple Master Ring

This is another form of ring topology, where there are multiple masters on the ring, and these masters have to receive data as well as transmit data to the next master. In the most complex case, each node is a master, which means that it receives data from the previous master and sends data to the next master. Flow control is not allowed in this topology for rings above two nodes, and the data cannot be passed through masters unless control guarantees that there is at least one source-only node on the ring and that no two masters will transmit at the same time. Single master rings should temporarily become multiple master rings when switching loop masters.

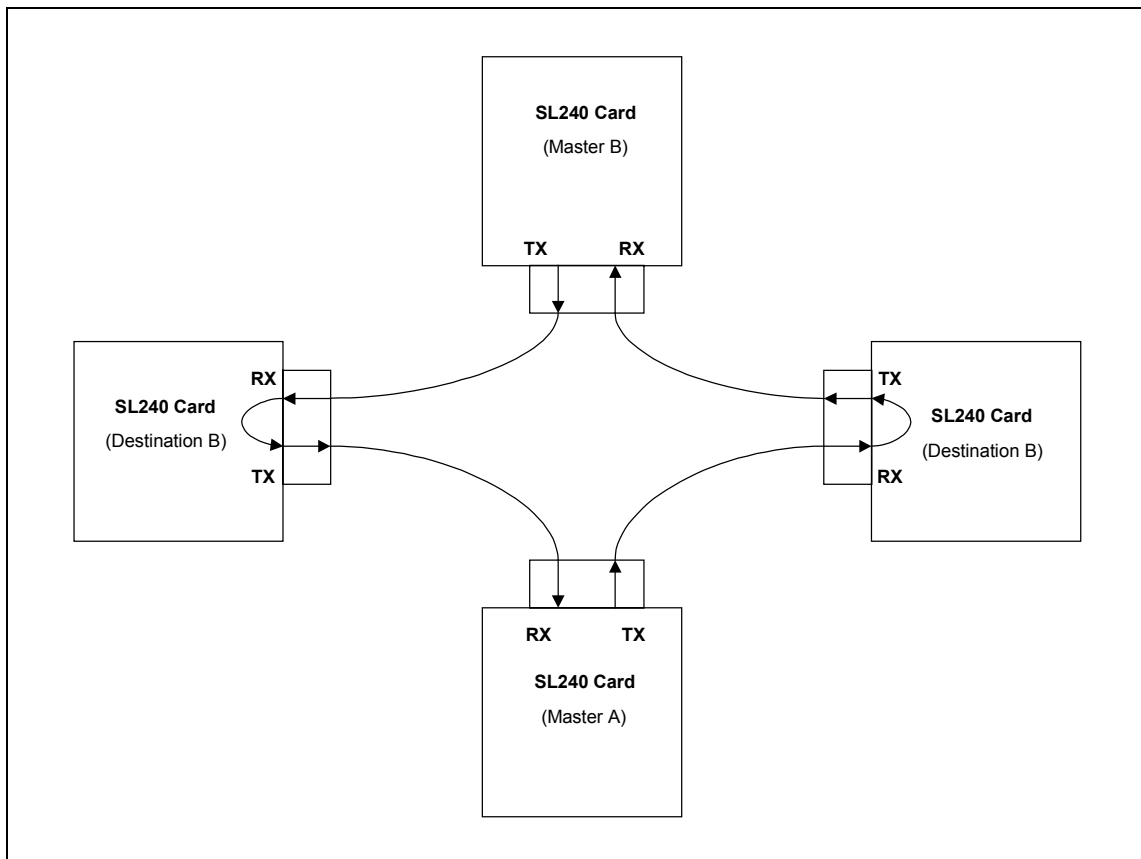


Figure 2-11 Multiple Master Ring

2.5 Status “LINK UP” LED

All of the SL240 cards are equipped with a link status indicator LED. This LED is labeled “LINK UP.” When this LED is illuminated, it indicates a signal is present on the receiver. This LED gives no indication of the validity of the signal, only that a signal is present.

3. INSTALLATION

3.1 PCI, PMC, and CPCI Installation Procedures

SL240 cards require only one slot on the host computer backplane and interface directly to fiber-optic transmission media.

To install an SL240 card, follow the steps below:

1. Unpack the card.
2. Inspect the card.
3. Install the card.
4. Connect the cables.

3.2 Unpack the Cards



CAUTION: Exercise care regarding the static environment. Use an anti-static mat connected to a wristband when handling or installing the SL240 card. Failure to do this may cause permanent damage to the components on the card.

Follow the steps below to unpack the card:

1. Put on the wristband attached to an anti-static mat.
2. Remove the card and anti-static bag from the carton.
3. Place the bag on the anti-static mat.
4. Open the anti-static bag and remove the card.
5. In the unlikely event that you should need to return your SL240 card, please keep the original shipping materials for this purpose.

Any optional equipment is shipped in separate cartons.

3.3 Inspect the Cards

The SL240 card consists of a single card with a built-in link interface. If the card was damaged in shipping, notify Systran Corporation or your supplier immediately.

3.4 Install the Cards



WARNING: Turn off all power to your operating system before attempting to install the SL240 Cards.

3.4.1 SL240 PCI Card

To install the SL240 PCI card, push the card into the mother board, as shown in Figure 3-1, steps 1 and 2, until it is firmly seated. Install the mounting screw as shown in step 3.

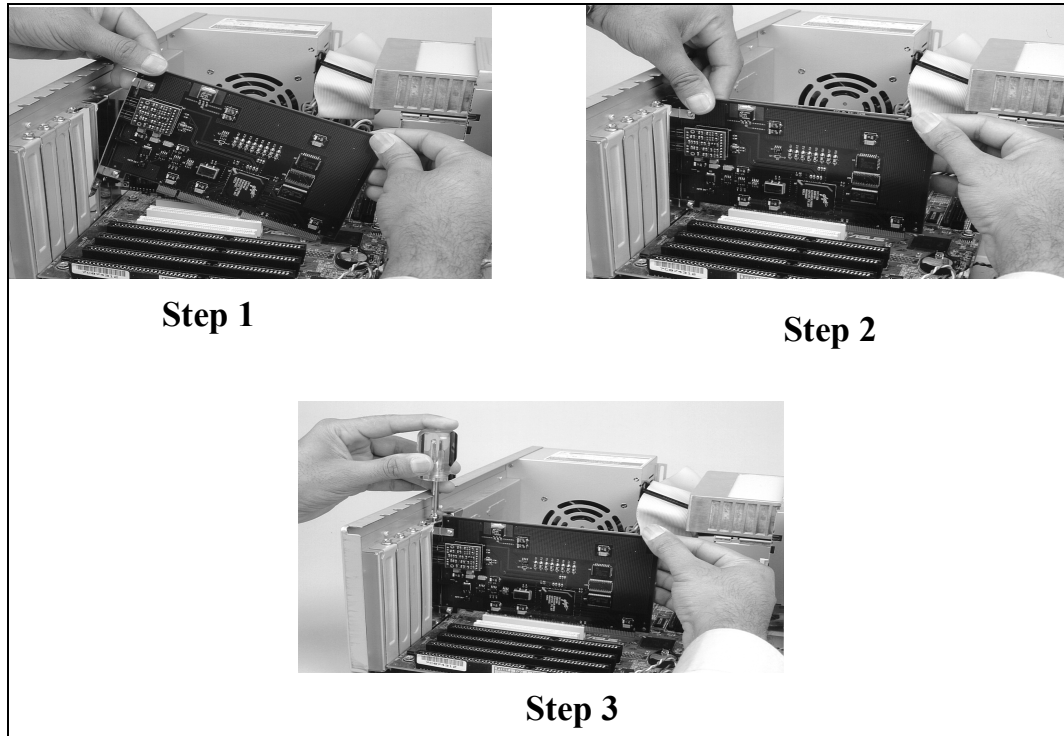
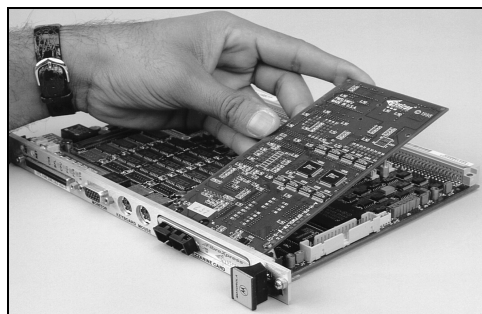


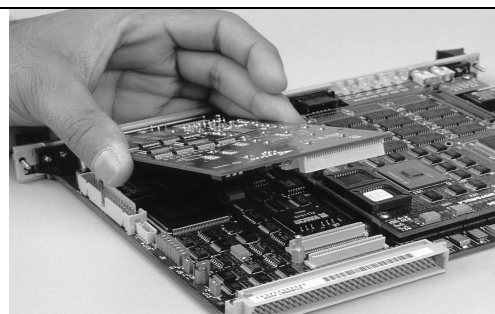
Figure 3-1 SL240 PCI Card Installation

3.4.2 SL240 PMC Card

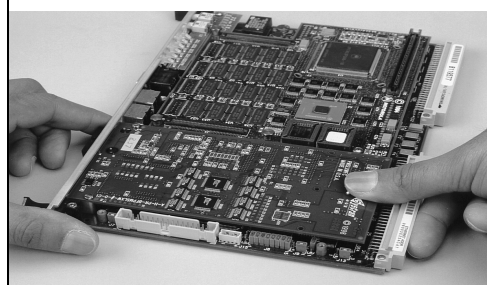
To install the SL240 PMC card, insert the card into an available slot by pushing the faceplate into the cutout on the carrier until it butts up against the mating connector as shown in Figure 3-2, steps 1 and 2. Then firmly push the connectors together. Install the four mounting screws through the PCB of the host SBC to fasten it in place, as shown in step 3.



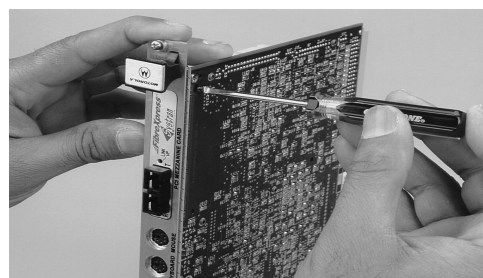
Step 1 (Viewed from Front)



Step 1 (Viewed from rear)



Step 2



Step 3

Figure 3-2 SL240 PMC Card Installation

3.4.3 SL240 CPCI Card

To install the SL240 CPCI card, push the card into the mother board, as shown in Figure 3-3, until it is firmly seated (step 1), then install the mounting screw (step 2).

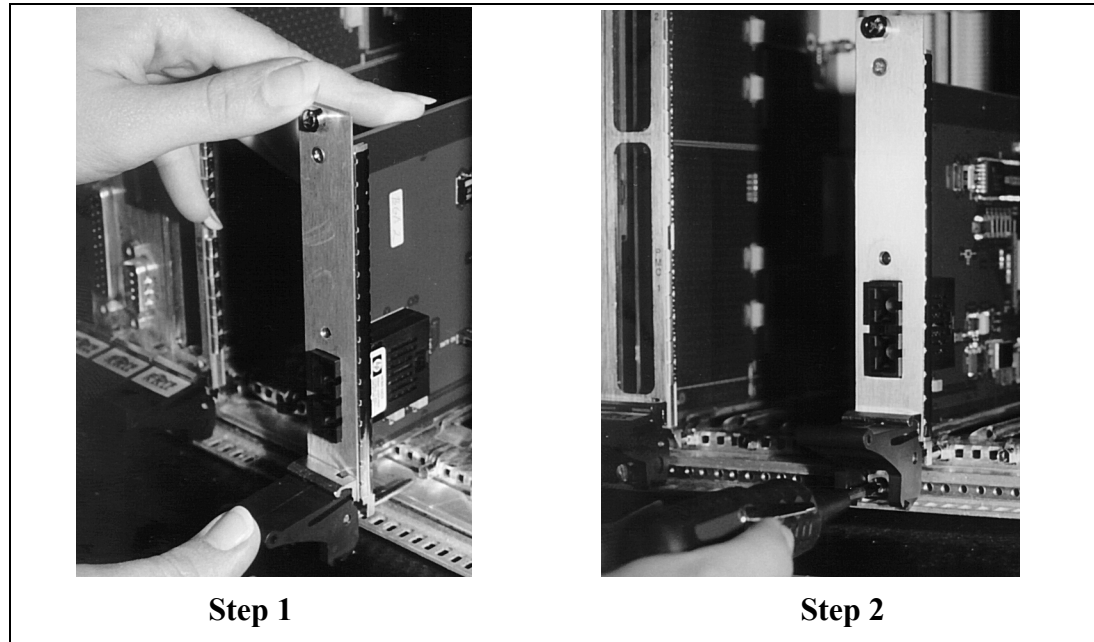


Figure 3-3 SL240 CPCI Card Installation

3.5 Connect the Cables

3.5.1 Transmission Media

For short wavelength laser modules, either a 50 μm or 62.5 μm core diameter cable should be used. For distances up to 300 meters 62.5 μm can be used. 50 μm cable allows distances up to 500 meters. For distances greater than 500 meters, (up to 10 kilometers,) long wavelength laser modules with 9 μm core cable should be used.

3.5.2 Fiber-optic Cables

The two factors to consider when connecting the cables are the topology and the transmission media used. The cards can be connected in several different topologies depending on your application. See section 2.4, Topologies, for more detailed examples.



Fiber-optic Cable Precautions

CAUTION: Fiber-optic cables are made of glass and may break if crushed or bent in a loop with less than a 2-inch radius.

Look at the cable ends closely before inserting them into the connector. If debris is inserted into the transmitter/receiver connector, it may not be possible to clean the connector out and could result in damage to the transmitter or receiver lens. Hair, dirt, and dust can interfere with the light signal transmission.

Use an alcohol-base wipe to clean the cable ends.

For short wavelength laser modules, either a 50 μm or 62.5 μm core diameter cable should be used. For distances up to 300 meters 62.5 μm can be used. 50 μm cable allows distances up to 500 meters. For distances greater than 500 meters (up to 10 kilometers), long wavelength laser modules with 9 μm core cable should be used.

The optional fiber-optic cables may be shipped in a separate carton. Remove the rubber boots on the fiber-optic transmitters and receivers as well as the ones on the fiber-optic cables. Replace these rubber boots when cables are not in use or if the node must be returned to the factory. Attach the fiber-optic cables to the connectors on the SL240 card.

Figure 3-4 and Figure 3-5 depict the types of fiber-optic connectors needed for the SL240 card.

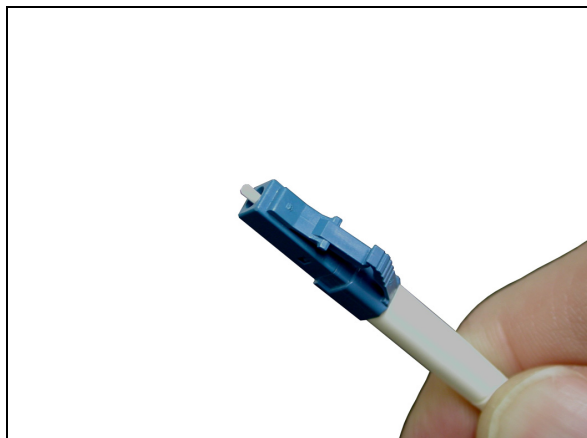


Figure 3-4 Fiber-optic Simplex LC Connector

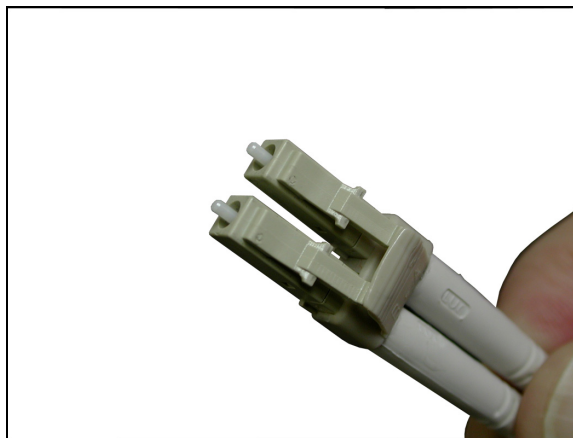


Figure 3-5 Fiber-optic Duplex LC Connector

3.5.3 Copper Cables

HSSDC connectors use the 150 ohm duplex, shielded quad-type copper cable. The maximum distance of this media is 30 meters. Figure 3-6 is a representation of the HSSDC connector and receptacle.

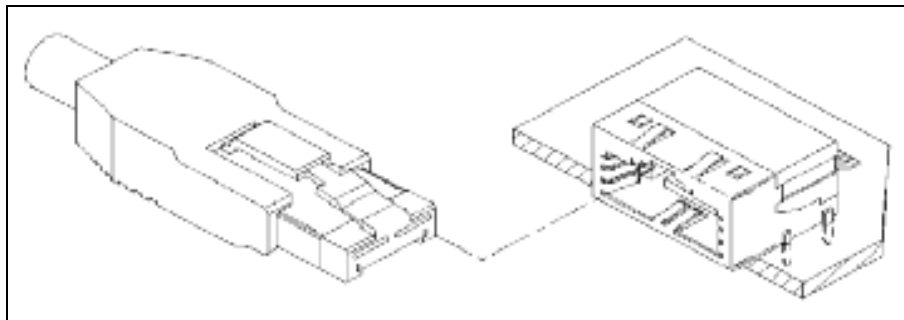


Figure 3-6 HSSDC Connector and Receptacle

3.6 Troubleshooting

If the system does not boot correctly, power down the machine, reseal the card, double-check cable connections, and turn the system back on. If problems persist, contact Systran Technical Support at **(800) 252-5601** or **support@systran.com** for assistance.

Please be prepared to supply the following information:

Machine: _____
OS Name: _____
OS Version: _____
Card Type: _____
Card Serial #: _____
Software Part #: _____
Software S/N: _____
Problem Reproducibility: _____
Problem Description: _____

4. OPERATION

4.1 Overview

SL240 cards move data with very low latency from a host interface to or from a 2.5 Gbps link. The host interfaces available are an FPD²-like proprietary interface and a PCI interface. The advantage of the FPD²-like interface is that it requires very simplistic hardware to interface. The PCI interface will interface with any standard PCI bus, and therefore has many advantages for portability at the cost of some software overhead.



CAUTION: Do **not** break the link between two SL100 boards. Unpredictable results may occur that could affect your system.

4.2 Theory of Operation

The operation of SL240 cards is simple—take data from the host bus interface and transmit it across a link, or take data from the link and pass it to the host bus interface. The link protocol involved is kept minimal to reduce the latency and improve throughput, while still providing a set of useful features with which to customize your applications. The hardware offers many different features for advanced applications, while maintaining a simple interface to the most commonly used features.



NOTE: For further explanation of terms used in the following sections, consult the FPD² Primer in Appendix F.

4.2.1 Receive Operation

The SL240 card has several options for receiving data. The most basic option is no-loop operation with data-receive enabled. In this case, data is:

1. Received from the link.
2. Decoded by the card.
3. Placed in the receive FIFO.

At this point, the operation depends on the host interface.

If it is a PCI-based card and a receive DMA is started, the data is automatically moved into the PCI address given by the DMA transaction. If no DMA is started, the data waits in the receive FIFO until the host either PIOs the data out or sets up the DMA transaction to remove it.

If it is an FPD²-based card, and /SUSPEND is not asserted, the card asserts /DVALID and proceeds to transmit the data on the FPD² interface. If /SUSPEND or /NRDY is asserted, then the data waits in the receive FIFO until these signals go away. The maximum delay from the link to the bus interface is 1.5 μ s for SL100 or 500 ns for SL240.

FPD² signals are embedded into the control words of a frame. The FPD² signals transported across are: /NRDY, /DIR, /SYNC, PIO1 and PIO2. A /SUSPEND signal is synthesized by the transmit state machine in response to how full the receive FIFO is—this is not the /SUSPEND from an FPD² port.

All FPDP signals, with the exclusion of /SYNC, are passed around the receive FIFO, and are not synchronized with the data stream. For PCI variations of this card, the FPDP signals can be read from a register once they are received from the link.

4.2.2 Transmit Operation

The transmit operation first has to collect data in the transmit FIFO for transmission. On PCI-based cards, this means that either data is PIO'd into the transmit FIFO or a DMA transaction is set up to fill the FIFO. FPDP cards collect any data words accompanied by /DVALID on the FPDP interface. Once a data word is in the FIFO, transmission can begin. The framing-state machine first checks that there is no data in the retransmit FIFO and that the remote node is not telling this node to back off. If it is clear to send, after it transmits the next SOF it will begin filling the data frame as full as possible (up to 2048 bytes). The data is then encoded and sent out across the link. If there is data in the retransmit FIFO or the card is being backed off from the destination, then the card waits until both conditions are clear before it starts transmission. The maximum delay for the first data word from the bus interface to the link is 1.5 μ s for SL100 or 500 ns for SL240 when it is not being backed off.

All FPDP signals, with the exclusion of /SYNC, are passed around the transmit FIFO, and are not synchronized with the data stream. For PCI variations of this card, the FPDP signals can be written to a register and then transmitted across the link.

4.2.3 Loop Operation

Loop operation on SL240 acts like a virtual FPDP bus, where one source (the loop master) transmits to any number of receive nodes. The link protocol is the same for this operation, except for any node in the loop may assert the /SUSPEND or /NRDY signals embedded in this data stream. This implies that if one node on the loop is not ready to receive data, the source is backed off for all nodes. This is the same way that multi-drop FPDP busses function. The difference is that the /NRDY signal is not used to back off the loop master—it is only used for status information. /SUSPEND is the only signal capable of backing off the loop master.

The fundamental difference between a loop master and a receiving node is that the loop master does not have its loop retransmission enabled. So, to the loop master, it appears as if it is still in a point-to-point connection with a single node. Receiving nodes, on the other hand, have knowledge that they are in a loop configuration, and must be configured as such. Note that the loop master receives all the data that it transmits, so data can either be checked for errors or ignored when it is received. This checking (beyond CRC checking) is not done on the SL240 card, and must be implemented by the system designer.

The receivers on the loop can choose to collect the data or ignore it. This option is configured through software. If the receive FIFO is enabled (the node is collecting data), the /SUSPEND and /NRDY signals may be asserted by this node as the data passes through. If it is not configured to receive the data, it simply passes the data through without modifying /NRDY or /SUSPEND.



NOTE: One node on the loop **MUST** be in non-loop operation in order for loop operation to work correctly. One node needs to remove the data from the loop. When switching masters on the loop, both the previous master and the next master should be in non-loop operation before the previous master switches into loop mode.

4.3 Data Synchronization

There is a data synchronization primitive, called /SYNC, which is sent across the link under user control. This primitive synchronizes with the data stream. On the PCI variations of SL240, this is written to the transmit FIFO under user control or through the transaction channels. On the FPDP variations of the card, this signal is the /SYNC line on the FPDP interface.

The /SYNC on PCI devices corresponds to /SYNC without /DVALID on the FPDP interface. The only /SYNC that will be sent to the status registers on PCI is /SYNC without /DVALID. There is an option to convert /SYNC with /DVALID from FPDP sources into /SYNC without /DVALID on PCI cards, so all /SYNC primitives can be received by the PCI variations of SL240.

4.4 Configuration Options

There are many different configuration options available which affect the operation of the SL240 card. Most of these options are configured in the Link Control register (described in Appendix B).

4.4.1 Flow Control

Flow control allows a receiver to throttle the data stream from a transmitter. If this option is turned off, the card will continue to send data even when the receiver signals it to stop. This may be a desirable option if late data is useless and you do not wish to back off the transmitter.

The other option that flow control infers is how the card behaves when the link is down. The default operation with flow control enabled stops the transmitter when the link is down. With the card set to ignore flow control, the card will still transmit with the receive fiber removed. This is useful for single-fiber systems where flow control is unimportant and data is moving only in one direction.

4.4.2 Loop Enable

The loop-enable option allows the SL240 card to transmit the received data stream again. Turning on the loop enable implies that this node is designated as a receiver in the current configuration.

4.4.3 Receiver/Transmitter Enable

The transmitter-enable and receiver-enable bits in the Link Control register turn off the transmit and receive data streams, respectively. Neither affects the loop operation, so data will still be retransmitted if the loop operation is enabled. This makes these options useful for record/playback systems where you wish to merely retransmit the data received without processing it. The receive-enable is useful for disabling the receive FIFO for the master in loop operation so that the data sent is not received.

4.4.4 CRC Generation/Checking

The CRC Generation/Checking option allows the SL240 card to detect data transmission errors. The card is not capable of correcting the errors. Error correction is left to application level software.

This single bit controls both generation and checking. This means that all nodes on the loop (or on both sides of a point-to-point configuration) must be configured exactly the same. Failure to configure them the same will mean excessive CRC errors for one end and extra data for the other.

4.4.5 Stop on Link Error or /SYNC

There are two DMA stop conditions available to the user—stop on link error and stop on /SYNC. The stop on link error stops the DMA engine from removing data from the receive FIFO when there is a link error, such as the link going down. The stop on /SYNC option allows you to stop data from being received from the receive FIFO when a /SYNC without /DVALID is received on the output.



NOTE: The Watchdog Timer and Receive FIFO Threshold Interrupt features discussed below are not available in the current revision of the firmware. However, they will be made available in a future revision. When released, they will operate as described in the manual.

4.4.6 Watchdog Timer

SL240 cards have a watchdog timer, which can be set to disable the laser if the timer expires. This adds a powerful fault tolerance feature when the card is connected in a loop through an LinkXchange Crossbar Switch, which switches the card out of the loop when the laser turns off. The watchdog timer is reset through a simple control register write.

4.4.7 Receive FIFO Threshold Interrupt

SL240 cards can be configured to interrupt the host when the FIFO passes a certain threshold, allowing for efficient PIO transactions out of the receive FIFO. This is particularly important on data storage systems, where you do not want to remove data from the FIFO until you have a full block of data to transmit. One of 256 different thresholds is selected through the control registers.

APPENDIX A

SPECIFICATIONS

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A.1 Specifications

A.1.1 PCI Specifications

Physical Dimensions:	174.6 x 106.7 mm
Weight:	≈ 0.25 lbs
Operating Voltage:	4.75 V to 5.25 V
Power Dissipation:	8.5W
Operating Temperature Range:	+0° to +50°C
Operating Humidity Range:	5% to 95% (noncondensing)
Mean Time Between Failure (MTBF)*:	
Short wavelength laser:	93,609 hours (10.7 years)
Long wavelength laser:	90,230 hours (10.3 years)
Storage Temperature Range:	-40° to +85°C
Storage Humidity Range:	0% to 95% (noncondensing)

A.1.2 PMC Specifications

Physical Dimensions:	74.0 x 149.0 mm
Weight:	≈ 0.25 lbs
Operating Voltage:	4.75 V to 5.25 V
Component Density (Side View):	Side 1 – 90% (Max)** Side 2 – 90% (Max)**
Power Dissipation:	Side 1 — 7W Side 2 — 1.5W
Operating Temperature Range:	+0° to +50°C
Operating Humidity Range:	5% to 95% (noncondensing)
Mean Time Between Failure (MTBF)*:	
Short wavelength laser:	91,634 hours (10.5 years)
Long wavelength laser:	88,394 hours (10.1 years)
Storage Temperature Range:	-40° to +85°C
Storage Humidity Range:	0% to 95% (noncondensing)

A.1.3 CPCI Specifications

Physical Dimensions:	3U – 160 x 100 mm 6U – 160 x 233 mm
Weight:	≈ 0.25 lbs
Operating Voltage:	4.75 V to 5.25 V
Power Dissipation:	Side 1 — 7W Side 2 — 1.5W
Operating Temperature Range:	+0° to +50°C
Operating Humidity Range:	5% to 95% (noncondensing)
Mean Time Between Failure (MTBF)*:	
Short wavelength laser:	134,531 hours (15.4 years)
Long wavelength laser:	134,458 hours (15.3 years)

Storage Temperature Range: -40° to +85°C

Storage Humidity Range: 0% to 95% (noncondensing)

* The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A, for a ground-benign environment.

** These values are calculated estimates.

A.2 Media Interface Specifications

A.2.1 SL100 Media Interface Specifications

Connector:Duplex LC

850 nm:

Media50 µm or 62.5 µm multimode fiber

Fibre Channel Formats:100-M5-SN-I (1 Gbps, 50 µm fiber)

100-M6-SN-I (1 Gbps, 62.5 µm fiber)

Maximum Fiber Length:500 meters with 50 µm fiber

300 meters with 62.5 µm fiber

Transmit Wavelength:830 to 860 nm

Transmit Power:-10 to -4 dbm

Receive Wavelength:770 to 860 nm

Receive Sensitivity:-16 to 0 dbm

1300 nm:

Media9 µm single-mode fiber*

Fibre Channel Formats:100-SM-LL-I (1 Gbps, single-mode fiber,
intermediate distance)

100-SM-LC-L (1 Gbps, single-mode fiber, low
cost long distance)

Maximum Fiber Length:10 km

Transmit Wavelength:1285 to 1330 nm

Transmit Power:-9 to -3 dBm

Receive Wavelength:1100 to 1600 nm

Receive Sensitivity:-20 to -3 dBm

* (1300 nm cards are also usable with multimode fiber.)

A.2.2 SL240 Media Interface Specifications

Connector:Duplex LC

850 nm:

Media50 µm or 62.5 µm multimode fiber

Maximum Fiber Length:150 m with 50 µm fiber

100 m with 62.5 µm fiber

Transmit Wavelength:830 to 860 nm

Transmit Power:-8 to -4 dbm

Receive Wavelength:770 to 860 nm

Receive Sensitivity:-12 to 0 dbm

1300 nm:

Media9 µm single-mode fiber

Maximum Fiber Length:10 km

Transmit Wavelength:1285 to 1335 nm

Transmit Power:-7.5 to -3 dBm

Receive Wavelength:1270 to 1355 nm

Receive Sensitivity:-18 to -3 dBm

A.2.3 HSSDC Copper Media Interface

Cable:	150 Ohm shielded, Quad
Maximum Cable Length:	Up to 30 meters with equalized cable Up to 25 meters with non-equalized cable
Compatibility:	100-TW-EL-S (1 Gbps, shielded, balanced cable)
Connector:	HSSDC (Fibre Channel “Style-2”)
Data Rate:	1.0625 Gbps or 2.5 Gbps

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APPENDIX B

REGISTER SET

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B.1 Overview



NOTE: The FibreXtreme SL100 and SL240 PCI, PMC, and CPCI Cards will be referred to throughout this appendix as PCI. Anything that is exclusive to the PCI, PMC, or CPCI Cards will be described as such.

The PCI SL240 card is very easy to program. With minimal programming, the PCI SL240 card can transfer data between PCI hosts. This section details the actual bit definitions to the registers, which are explained in Appendix C (SL100/SL240 Programming).



NOTE: In some cases, the Receive FIFO Threshold register shows data in the FIFO, but attempts to clear that data by reading from the FIFO fail.

B.2 Accessible resources

There are three accessible resources on the PCI SL240 card—PCI Configuration registers, the runtime register set, and the FIFO. The mechanisms for accessing these are platform specific and therefore outside the scope of this document, though the contents are detailed here.

B.3 PCI Configuration registers

The PCI SL240 card contains a standard PCI configuration space header, with the device ID of 0x4640 and the vendor ID of 0x1387. There are also two base addresses initialized for the card – the first is a 256 byte space representing the runtime registers, the second is a one-megabyte space reserved for the FIFO.

B.4 Runtime Register set

The runtime register set is accessed through 32-bit memory accesses to the Base Address 0 from PCI Configuration space. These registers represent all of the configuration, control, and status registers for the PCI SL240 card. Table B-1 shows the layout of these registers in PCI space.

B.4.1 Bit Definitions

- **R/W** – Readable/Writable bit
- **R/WOC** – Readable/Write One to Clear bit
- **W** – Write-only bit
- **R** – Read-only bit

Table B-1 SL240 Register Layout

	REGISTER LAYOUT	
	4	0
0x00	Board CSR	Interrupt CSR
0x08	Link Status	Link Control
0x10	Receive FIFO Threshold	FPDP Flags
0x18	Reserved	Watchdog Timer
0x20	Reserved	Queue Address 0
0x28	Reserved	Queue Control 0
0x30	Transaction Length 0	Transaction CSR 0
0x38	Reserved	Reserved
0x40	Reserved	Chain PCI Address 0
0x48	Next Chain Entry 0	Chain Length/Flags 0
0x50	Reserved	Queue Address 1
0x58	Reserved	Queue Control 1
0x60	Transaction Length 1	Transaction CSR 1
0x68	Reserved	Reserved
0x70	Reserved	Chain PCI Address 1
0x78	Next Chain Entry 1	Chain Length/Flags 1
0x80	Reserved	
0x88		
0x90		
0x98		
0xA0		
0xA8		
0xB0		
0xB8		
0xC0		
0xC8		
0xD0		
0xD8		
0xE0		
0xE8		
0xF0		
0xF8		

B.4.2 Interrupt CSR (INT_CSR)—Offset 0x00

Field	Description	Access	Reset Value
0	Transaction Channel 0 Interrupt Active – ‘1’ if active, ‘0’ if not active. Write ‘1’ to clear.	R/WOC	0
1	Transaction Channel 1 Interrupt Active – ‘1’ if active, ‘0’ if not active. Write ‘1’ to clear.	R/WOC	0
2	DMA Chain 0 Interrupt Active – ‘1’ if active, ‘0’ if not active. Write ‘1’ to clear.	R/WOC	0
3	DMA Chain 1 Interrupt Active – ‘1’ if active, ‘0’ if not active. Write ‘1’ to clear.	R/WOC	0
4	Link Error Interrupt Active – ‘1’ if active, ‘0’ if not active. Write ‘1’ to clear.	R/WOC	0
5	FPDP Interrupt Active – ‘1’ if active, ‘0’ if not active. Write ‘1’ to clear.	R/WOC	0
6	Threshold Interrupt – ‘1’ if active, ‘0’ if not active. Write ‘1’ to clear.	R/WOC	0
7	Watchdog Interrupt – ‘1’ if active, ‘0’ if not active. Write ‘1’ to clear.	R/WOC	0
15 to 8	Reserved.	None	0
16	Enable Transaction Channel 0 Interrupt – ‘1’ to enable interrupts, ‘0’ to disable.	R/W	0
17	Enable Transaction Channel 1 Interrupt – ‘1’ to enable interrupts, ‘0’ to disable.	R/W	0
18	Enable DMA Chain 0 Interrupt – ‘1’ to enable interrupts, ‘0’ to disable.	R/W	0
19	Enable DMA Chain 1 Interrupt – ‘1’ to enable interrupts, ‘0’ to disable.	R/W	0
20	Enable Link Error Interrupt – ‘1’ to enable interrupts, ‘0’ to disable.	R/W	0
21	Enable FPDP Interrupt – ‘1’ to enable interrupts, ‘0’ to disable.	R/W	0
22	Enable Threshold Interrupt – ‘1’ to enable interrupts, ‘0’ to disable.	R/W	0
23	Enable Watchdog Interrupt – ‘1’ to enable interrupts, ‘0’ to disable.	R/W	0
31 to 24	Reserved.	None	0

B.4.3 Board CSR (BRD_CSR)—Offset 0x04

Field	Description	Access	Reset Value
0	Little Endian – Set to '1' for unswapped control registers. Setting to '0' has no effect.	R/W	1
1	Reset – Write '1' to reset the board. Writing '0' has no effect.	W	0
2	Swap data bytes – Set to '1' to 32-bit swap the data transferred through PIO transactions. '0' for unswapped transactions.	R/W	0
3	JTAG TCK# - Controls the TCK# line on the JTAG port.	R/W	0
4	JTAG TMS# - Controls the TMS# line on the JTAG port.	R/W	0
5	JTAG TDO# - Controls the TDO# line on the JTAG port.	R/W	0
6	JTAG TDI# - TDI# line from the JTAG port.	R	1
7	JTAG Enable – Enable the JTAG port on the FPGA.	R/W	0
13 to 8	Revision ID – Revision level of the board controller.	R	See desc.
14	3.3 V/5 V PCI Signaling - '1' indicates the SL100/SL240 card uses 3.3 V PCI signaling '0' indicates the SL100/SL240 card uses 5 V PCI signaling	R	See desc.
15	SL100/SL240 – '1' if this is an SL240 board, '0' for SL100.	R	See desc.
23 to 16	Reserved.	R	0
24	Big Endian – Set to '1' to swap the control registers. Set to '0' for Little Endian.	R/W	0
25	64-bit transaction disable – '1' to disable 64-bit transactions, '0' to enable 64-bit transactions	R/W	0
26	Swap words – Set to '1' to swap words within a 64-bit transaction. Set to '0' for no swapping.	R/W	0
31 to 27	Reserved.	None	0

B.4.4 Link Control (LINK_CTL)—Offset 0x08

Field	Description	Access	Reset Value
0	Allow Remote Transmitter – Set to '1' to allow the remote transmitter on the link to send data. Set to '0' to suspend the remote transmitter on the link from sending data.	R/W	0
1	CRC Enable – Set to '1' to enable CRC checking/generation. Set to '0' to disable.	R/W	0
2	Ignore Flow Control – Set to '1' to ignore flow control from the remote end and continue transmitting when the link is down. Set to '0' to stop transmission when the link goes down or the remote end on the link interface is sending a back-off signal to the transmitter card.	R/W	0
3	Convert SYNC – When set, a SYNC without DVALID is appended after every SYNC with DVALID from the link.	R/W	0
4	Stop on SYNC without DVALID – If '1' then stop the receive FIFO until software re-enables the transaction. If '0' the receive FIFO is not stopped.	R/W	0
5	Stop on receiver error – If '1' then the receive FIFO is stopped when a CRC error or FIFO overflow is taken out of its output. If '0', the receive FIFO is not stopped.	R/W	0
6	SYNC as D0 – If '1', bit 0 of the data stream is used as /SYNC in the outgoing and incoming data stream. If '0', bit 0 is not used as /SYNC.	R/W	0
7	Reserved	None	0
8	Disable Receiver – '1' disables the link interface from placing data in the receive FIFO. '0' for normal receive operation.	R/W	0
9	Disable Transmitter – '1' disables the link interface from removing things from the transmit FIFO. '0' for normal transmit operation.	R/W	0
10	EWRAP – This signal controls loopback operation of the user interface's data stream. A '1' indicates the outgoing data stream is electronically wrapped into the incoming data stream at the serializer/deserializer. A '0' indicates non-wrapped data flow to and from the link interface.	R/W	0

Continued on next page.

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11	LWRAP – This signal controls loopback operation of the link interface's data stream. A '1' indicates the incoming data stream is electronically wrapped into the outgoing data stream at the FPGA. A '0' indicates non-wrapped data flow to and from the user interface.	R/W	0
15 to 12	Reserved	None	0
16	Reset SR – Write '1' to clear any latched status information from the registers. Writing '0' has no effect.	W	0
17	Clear SYNC without DVALID – Write '1' to release a FIFO stopped on SYNC without DVALID. Writing '0' has no effect.	W	0
18	Clear Receiver Error – Write '1' to release a FIFO stopped on a receiver error condition. Writing '0' has no effect.	W	0
19	Erase TX FIFO – Write '1' to clear the transmit FIFO. Writing '0' has no effect.	W	0
20	Erase RX FIFO – Write '1' to clear the receive FIFO. Writing '0' has no effect.	W	0
31 to 21	Reserved	None	0

B.4.5 Link Status (LINK_STAT)—Offset 0x0C

Field	Description	Access	Reset Value
7 to 0	8B10B Errors – 8 bit counter counting the current number of 8B10B decoding errors discovered. Cleared through 'Reset SR' in LINK_CTL.	R	0x00
8	Link Down – A '1' indicates the link has gone down at some point since the last 'Reset SR'. A '0' indicates the link has not gone down since the last 'Reset SR'. This bit is cleared through 'Reset SR' in LINK_CTL.	R	0
9	Link Up – This bit reflects the current status of the link. A '1' indicates the link is currently up. A '0' indicates the link is currently down. Note that this bit is not latched like the 'Link Down' bit.	R	0
10	Synchronization Error – A '1' indicates the card has corrected a synchronization error on the incoming data stream. A '0' indicates the card has not corrected a synchronization error on the incoming data stream. This bit is cleared through 'Reset SR' in LINK_CTL.	R	0
11	Checksum Error – A '1' indicates the card has detected a checksum error on the incoming data stream. A '0' indicates the card has not detected a checksum error on the incoming data stream. This bit is cleared through 'Reset SR' in LINK_CTL.	R	0
12	RX FIFO Overflow - A '1' indicates the receive FIFO has overflowed. A '0' indicates the receive FIFO has not overflowed. This bit is cleared through 'Reset SR' in LINK_CTL.	R	0
13	TX FIFO Overflow – A '1' indicates the transmit FIFO has overflowed. A '0' indicates the transmit FIFO has not overflowed. This bit is cleared through 'Reset SR' in LINK_CTL.	R	0
31 to 14	Reserved	None	0

B.4.6 FPDP Flags (FPDP_FLGS)—Offset 0x10

Field	Description	Access	Reset Value
0	Send SYNC – Write ‘1’ to send SYNC without DVALID. Writing ‘0’ has no effect.	W	0
1	PIO1 Out – State of the PIO1 line sent across the link.	R/W	0
2	PIO2 Out – State of the PIO2 line sent across the link.	R/W	0
3	DIR Out – State of the DIR line sent across the link.	R/W	0
4	NRDY Out – State of the NRDY line sent across the link.	R/W	0
7 to 5	Reserved.	None	0
8	SYNC Received – ‘1’ if a SYNC without DVALID has been received. Cleared through ‘Clear SYNC’ in the LINK_CTL register. ‘0’ if no SYNC has been received.	R	0
9	PIO1 In – State of the PIO1 line received from the link.	R	0
10	PIO2 In – State of the PIO2 line received from the link.	R	0
11	DIR In – State of the DIR line received from the link.	R	0
12	NRDY In – State of the NRDY line received from the link.	R	0
31 to 13	Reserved.	None	0

B.4.7 Receive FIFO Threshold—Offset 0x14

Field	Description	Access	Reset Value
19 to 0	Number of 32-bit words in the Receive FIFO.	R	0
20	Rearm Threshold Interrupt – Write ‘1’ to rearm the threshold register. Writing ‘0’ has no effect.	W	0
21	Data present – ‘1’ if data is present on the output. ‘0’ if no data is present.	R	0
23 to 22	Reserved.	None	0
31 to 24	Interrupt Threshold – Selects one of 256 divisions of the receive FIFO to interrupt on. 0x00 is when the FIFO has any data, 0xFF is when the FIFO is full.	R/W	0

B.4.8 Watchdog Timer—Offset 0x18

Field	Description	Access	Reset Value
23 to 0	Watchdog timer – Timer count in increments of 19.3 ns (SL100) or 8.2 ns (SL240).	R/W	0
24	Reset watchdog timer – Write '1' to reset the watchdog timer. Writing '0' has no effect.	W	0
25	Shutdown on timeout – Set to '1' to shutdown the laser on a watchdog timer timeout. Set to '0' for normal operation.	R/W	0
26	Manual laser shutdown – Set to '1' to shutdown the laser. Set to '0' for normal operation.	R/W	0
31 to 27	Reserved.	None	0

B.4.9 Transaction Channel 0 (Write Channel)

Queue Address (QADDR0)—Offset 0x20

Field	Description	Access	Reset Value
1 to 0	Reserved – Write as '0'	None	00
31 to 2	Bits 31 through 2 of PCI address for the transaction queue.	R/W	00

Queue Control (QCTL0) – Offset 0x28

Field	Description	Access	Reset Value
7 to 0	Producer Index for transaction queue.	R/W	0
15 to 8	Consumer Index for transaction queue.	R	0
23 to 16	Queue length – Place number of entries minus one here, where number of entries is a power of 2.	R/W	0
24	Enable Queue – ‘1’ enables the queue to fetch transaction entries. Setting this bit to ‘0’ pauses the transaction queue.	R/W	0
25	Reset Queue – Write ‘1’ to set the consumer and producer indices to 0 – Writing ‘0’ has no effect.	W	0
26	Abort Queue – Write ‘1’ to this bit to abort the current transaction pending on the transaction controller. Writing ‘0’ has no effect.	W	0
27	Stop on /SYNC – Set to ‘1’ to disable the controller on /SYNC received (receive side only). Set to ‘0’ for normal operation.	R/W	0
28	Stop on link error – Set to ‘1’ to disable the controller on link errors. Set to ‘0’ for normal operation.	R/W	0
29	Queue paused – ‘1’ if the queue is paused, ‘0’ otherwise.	R	0
30	Entries Available – ‘1’ if there are entries in the queue to process. ‘0’ if there are no entries.	R	0
31	Preserve – When the register is written with this bit set, only the producer index is written.	W	0

Transaction CSR (TNS_CSR0) – Offset 0x30

Field	Description	Access	Reset Value
0	Interrupt enable – Set to '1' to enable an interrupt on this transaction. Set to '0' for normal operation.	R/W	0
1	Skip entry – skips to the next entry when this bit is set. Set to '1' to enable. Set to '0' for normal operation.	R/W	0
2	/SYNC status – status of the /SYNC line to the controller.	R	0
3	Link error status – status of the link error line to the controller. '1' = error, '0' = no error.	R	0
4	Abort & Writeback on /SYNC – Set to '1' to abort the current transaction and write the status back to the transaction entry in memory on /SYNC (receive side only). Set to '0' not to abort.	R/W	0
5	Abort & Writeback on Link Error – Set to '1' to abort the current transaction and write the status back to the transaction entry in memory on Link Error. Set to '0' not to abort.	R/W	0
7 to 6	Reserved.	None	0
8	Send a /SYNC after this transaction is finished (transmit side only). Set to '1' to send, set to '0' not to send.	R/W	0
31 to 9	Reserved.	None	0

Transaction Length (TLENGTH0)—Offset 0x34

Field	Description	Access	Reset Value
31 to 0	Transaction length in 32-bit words.	R/W	0

Chain PCI Address (CPCIADDR0)—Offset 0x40

Field	Description	Access	Reset Value
1 to 0	Reserved (Lower two bits of PCI address must be zero).	None	0
31 to 2	PCI address for the buffer to transmit/receive.	R/W	0

Chain Length/Flags (CLENFLGS0)—Offset 0x48

Field	Description	Access	Reset Value
23 to 0	Length of buffer in 32-bit words.	R/W	0
24	End Chain – Write ‘1’ to say this is the last chain entry. Write ‘0’ if it is not.	R/W	0
25	Reserved.	None	0
27 to 26	Data swapping – “00” for straight, “01” to swap bytes, “10” to swap 32-bit words, “11” to swap 32-bit words and bytes.	R/W	0
28	Reserved.	None	0
29	Interrupt – Write ‘1’ to interrupt on transfer complete, Write ‘0’ otherwise.	R/W	0
30	Go – ‘1’ to start this transaction, ‘0’ to stop it. If it is a chained transaction, the first action is to fetch the chain entry.	R/W	0
31	Done – ‘1’ if this channel is currently idle. ‘0’ if a DMA is in progress.	R	0

Next Chain Entry (CNEXT0)—Offset 0x4C

Field	Description	Access	Reset Value
1 to 0	Reserved (Lower 2 bits of PCI address must be zero).	None	0
31 to 2	PCI address for the next chain entry.	R/W	0

Transaction Channel 1 (Read Channel)—(0x50 to 0x7F)

This register map for channel 1 is identical to the register map for 0x20 to 0x4F.

B.4.10 Transmit/Receive FIFOs

The transmit FIFO and receive FIFO are the last accessible resource on the SL240 card. FIFOs can use any address in the range of the second PCI base address. All address information for the transaction is disregarded, and the type of transaction (read or write) determines the FIFO that is addressed.

APPENDIX C

SL100/SL240 PROGRAMMING

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C.1 Introduction

The PCI SL240 card is designed so that programming the card is as simple as possible. This section details how to program the card for a variety of applications.



NOTE: The FibreXtreme SL100 and SL240 PCI, PMC, and CPCI Cards will be referred to throughout this appendix as PCI. Anything that is exclusive to the PCI, PMC, or CPCI Cards will be described as such.

C.2 Initializing the Card

The first register to initialize on the card is the BRD_CSR register. The only action required to configure this register is to write a 0x00000001 to it. By writing this value, the card is automatically configured for properly swapped 32-bit accesses, regardless of the host's endian conversion built into the bridge. Then, the card can be set up for transactions.

The LINK_CTL register then must be initialized before data transfer can take place. Most of the options available in the LINK_CTL register are described in Chapter 4. After initializing this register data can be transferred through PIO transactions. Due to PCI performance characteristics, Systran recommends using the card's DMA engine to transfer the data instead.

The following code segment demonstrates setting the card up for CRC checked operation.

```
/* Set the proper register swapping */
FXSL240[BRD_CSR] = 1;
```

```
/* Initialize the board to receive and transmit data */
FXSL240[LINK_CTL] = ALLOW_REMOTE_TX | CRC_ENABLE;
```

C.3 Connecting and Enabling Interrupts

Though not necessary for operation, interrupts are a key element in maintaining throughput with the card on any given system. Interrupts are configured through the INT_CSR register.

There are eight interrupt sources on the card: transaction channel 0, transaction channel 1, DMA chain 0, DMA chain 1, Link Errors, FPDP, threshold and watchdog interrupts. Transaction channel interrupts are signaled when a transaction counter expires on a channel or a transaction is completed. DMA chain interrupts occur when a DMA chain completes and the interrupt on complete bit is set for the chain entry. Link Error interrupts occur when certain events (link down, etc.) occur. FPDP Interrupts occur when one of the FPDP signals coming in off the link change. Threshold interrupts occur when the receive FIFO passes the interrupt threshold given in the threshold register for the first time. Watchdog interrupts occur when the watchdog timer expires on the card.

The following code segment sets up the card for watchdog interrupts and transaction channel interrupts.

```
/* Set up the INT_CSR register */
```

```
FXSL240[INT_CSR] = WATCHDOG_ENA | TNS0_ENA | TNS1_ENA;
```

C.4 Taking the Card Off-Line

In order to take the card off-line and stop both transmitting and receiving data, change the ‘Allow Remote Transmitter’ bit in LINK_CTL to be a ‘0’, which stops the remote transmitter. Setting ‘Disable Receiver’ and ‘Disable Transmitter’ bits in the LINK_CTL register also stops the receive FIFO from filling up and the transmit FIFO from emptying onto the link.

The following code segment disables both the transmit and receive FIFOs.

```
/* Kill both the transmit and receive FIFOs */  
FXSL240[LINK_CTL] |= DISABLE_TX | DISABLE_RX;
```

C.5 Disabling Interrupts

The interrupts to the PCI bus are disabled in the same way they are enabled – through the upper 16-bits of the INT_CSR register. Each of the six interrupt sources has a enable bit in this register to either allow or disallow the interrupt to be passed to the PCI bus. To disable any interrupt source, set its respective bit to ‘0’.

The following code segment disables the watchdog and transaction channel 0 interrupts on the card.

```
/* Don't allow transmit channel or watchdog interrupts */  
FXSL240[INT_CSR] &= ~(TNS0_ENA | WATCHDOG_ENA);
```

C.6 Handling Interrupts

To handle an interrupt, the following steps have to be taken:

1. Check the INT_CSR register to see if we are the card that interrupted.
2. Write the INT_CSR register with the read value to clear the interrupt.

An example of how to handle a simple interrupt follows:

```
/* Interrupt service routine for SL240 */
void isr() {
    /* Get the interrupt status */
    unsigned int status = FXSL240[INT_CSR];

    /* Clear the interrupt - these bits are write one clear */
    FXSL240[INT_CSR] = status;

    /*
     * All board manipulations based on the interrupt are now complete -
     * the rest of the code is implementation specific
     */

    /* While there are interrupts left to process */
    while (status & 0xff) {
        /* If transaction interrupt, manipulate structures based on these */
        /* ADD TRANSACTION HANDLING CODE HERE */
        /* Handle DMA interrupts */
        /* ADD DMA HANDLING CODE HERE */
        /* Handle link errors */
        /* ADD ERROR HANDLING CODE HERE */
        /* Handle FPDP Interrupts */
        /* ADD FPDP INTERRUPT HANDLING HERE */

        /* Handle threshold interrupts */
        /* ADD THRESHOLD INTERRUPT HANDLING HERE */

        /* Handle Watchdog Interrupts */
        /* ADD WATCHDOG INTERRUPT HANDLING HERE */

        status = slxc[INT_CSR];
        slxc[INT_CSR] = status;
    };
};
```

C.7 Sending and Receiving via PIO Transactions



CAUTION: Sending and receiving through either programmed I/O (PIO) transactions or using some other DMA engine in the system is not recommended with the SL240 card. PCI transactions will be retried on the PCI bus if there is no space in the transmit FIFO and it is a write transaction, or if there is no data in the receive FIFO and it is a read transaction.

It cannot be emphasized enough how detrimental an effect this will have on PCI performance. A problem exists if the SL240 card is the only device on the PCI bus, because you cannot access the control/status register to clear interrupts when a transaction is pending that cannot complete. If other devices are on the PCI bus, this means that they may or may not be able to access the bus, depending on the PCI arbiter involved.

When using PIO transactions to the SL240 card, addresses do not matter as long as they are within the 1 MB address range. The base address to do the transactions to is given in the second PCI base address in configuration space. The following code segment sends three longwords to the remote node assuming there is a routine called *config_read()* for your operating system to read PCI **config** space and no memory mapping is necessary.

```
/* Get the base address of FXSL240 unit 0 - PCI_BASE1 = 0x14 */
pio_base = config_read(0x1387, 0x4640, 0, PCI_BASE1);

/* Map buffer into our memory space - OS specific */
/* Write the data */
ptr = (unsigned int *)pio_base;
ptr[0] = 0xEDB0B123;
ptr[1] = 0xDEADBEEF;
ptr[0] = 0x12345678;
```

C.8 Sending and Receiving via Single DMA Transactions

The procedure for setting up a single DMA transaction is simple—there are two registers that have to be written: the Chain PCI Address and the Chain Length/Flags register. The Chain PCI Address is written with the PCI address to move the data from or to. The Chain Length/Flags register is more complicated. It is a combination of the length of the buffer, which is the lower 24 bits of this register, and the flags, which are the upper eight bits of the register. For a single DMA entry, set the ‘Interrupt bit’ if you want an interrupt completion, and the ‘Go’ bit. The following code segment demonstrates moving 1 KWord (4 KB) from the receive FIFO into a user buffer located at 0x40000000.

```
/* Set up the PCI address */

FXSL240[CPCIADDR0] = 0x40000000;

/* Set up the length/flags register - Add in an interrupt on
completion as well */

FXSL240[CLENFLGS0] = 0x70000400;
```

C.9 Sending and Receiving via a Chained DMA Transaction

Chained DMA transactions require DMA chains to be set up in PCI space. The DMA chain entries in PCI space are as follows:

0x00	Chain PCI Address
0x04	RESERVED
0x08	Chain Length/Flags
0x0C	Next Chain Address

The Chain PCI Address and Chain Length/Flags are the same registers as in the single DMA transactions. The Next Chain Address is new, and it represents the pointer to the DMA chain entry. In order to start the DMA transaction, software should write the Next Chain Address with the start of the transaction, and then set the 'Go' bit, and the length of zero in Chain Length/Flags register.

If the length is zero, the first thing the DMA controller does is load the next DMA chain entry into the registers. At this point, the DMA transaction is executed based on the values currently in the registers. Typically, the 'Interrupt' bit in the Chain Flags/Length register is set only on the last entry. The 'Go' bit can be cleared out by a transaction channel abort or the by the user during a transaction, effectively stopping a transaction. The following flowchart shows the DMA controller operations during a typical transaction.

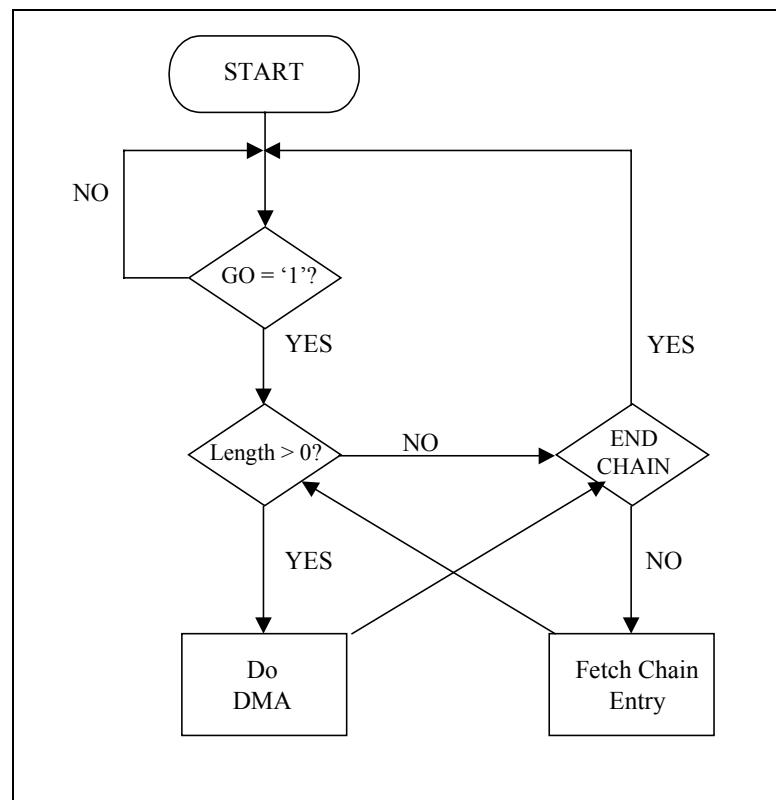


Figure C-1 DMA Controller Operations During Typical Transaction

C.10 Sending and Receiving via the Transaction Controllers

The transaction controllers offer a slightly different mechanism for transferring data. They use the DMA controllers in their operation, but they also allow you to enqueue /SYNC transactions as well. If the transmit transaction controller is used, it allows you to transmit /SYNC characters after a transaction finishes. If the receive transaction controller is used, it allows you to stop the transaction when a /SYNC is seen. The other feature of the transaction controller is that it allows you to post multiple requests to the device at a time. These requests each have their own DMA chain, and up to 256 requests can be posted with a single write to the PCI bus.

The transaction controllers are based on a queue structure. To initialize the controller, you have to set the queue base address and the queue control registers. All queue sizes used must be a power of two, and must be aligned on the size of the queue boundary. As each queue entry is four words, this means that a 16-entry queue would have to be aligned on a 256-byte boundary. The following code segment shows how to initialize the transaction controller for a 16-entry queue located at 0x40000000.

```
/* Set the queue address */
FXSL240[QADDR0] = 0x40000000;
/* Start the controller */
FXSL240[QCTL0] = (15<<16) | ENABLE_QUEUE;
```

Entries are posted to the controller through the producer index in the QCTL register. After the entry is written into memory, the user program should increment producer index by the number of entries added. The following code segment increments the register for posting four entries.

```
/* Post four entries to the queue */
tmp = FXSL240[QCTL0];
num_entries = 4;
FXSL240[QCTL0] = 0x80000000 | (tmp + num_entries);
```

Queue wrap-around is handled automatically in the controller (reading from entry 18 in a queue of length 16 will result in reading from entry 2).

The queue entries in memory consist of four words. The format is:

0x00	Transaction CSR
0x04	Transaction Length
0x08	(Status when written back)/RESERVED (write as '0')
0x0C	DMA Chain Start Address

The registers are loaded from the transaction entry once the producer index is updated—the TNS_CSR register is loaded from the first longword, the TLENGTH register is loaded from the second longword, and the DMA controllers CNEXT pointer is loaded from the fourth longword in the entry. When a register is written back (which can happen on link error or /SYNC for the receive side and on link down on the transmit side), the third word is the link status register. This allows the transaction to continue processing elements (if it is configured to do so) without waiting for the software to figure out what caused a link error.

C.11 Loop Operation

Loop operation with the SL240 card relies on out-of-band arbitration. For this reason, there is a small gap where no data transmissions should occur on the link when masters are switching. The loop master is always configured to not loop data back out. When switching to a new master, there should be a short time period where there are two masters on the loop. This way, it is guaranteed that the data flowing across the link will always be removed.

A limited form of in-band arbitration can be accomplished through various means. The first one is the FPD P PIO1 and PIO2 lines. /SYNC can also be used to switch masters if it is not used for other purposes.

The following code segment shows how to configure a node as the loop master without receive:

```
/* Start this card up as the loop master */
FXSL240[LINK_CTL]&= ~ LWRAP;
FXSL240[LINK_CTL] |= DISABLE_RX
And the change back to a receiver:
/* Make this node a receiver */
FXSL240[LINK_CTL] | LWRAP;
FXSL240[LINK_CTL] &= ~ DISABLE_RX
```

C.12 Sending and Receiving SYNC

There are many different options for sending and receiving synchronization signals from the link. Many of these methods are derived from the FPDP specification, and therefore have a close relationship to FPDP framing methods. The main methods of using SYNC are sending SYNC after a transaction and a programmed SYNC operation.

Sending SYNC without DVALID after a transaction is an option available through the transaction control (TNS_CSR) register. This allows a SYNC to be sent out on the link after a transmission finished. On the receive side, there are bits to stop the DMA transfer on SYNC and write the transaction entry data back into PCI space.

One item of note is that sending SYNC degrades the link performance, regardless of whether the sender is a PCI or CMC based card. If the FPDP frames (delimited by SYNC) are too small, they have a very negative effect on the throughput.

For the SL240 card (max throughput = 247 MB/s) and an FPDP frame size of n words ($n \leq 512$), the revised theoretical throughput is:

$$\text{throughput} = 247 \times \frac{n}{(n + 12)}$$

For a frame size of n for $n > 512$, with m equal to the number of whole frames transmitted ($m = n \text{ div } 512$).

$$\text{throughput} = 247 \times \frac{n}{[n + 6(m + 1)]}$$

For example, if the frame size is set to 2000 words, then:

$$m = (2000 \text{ div } 512) = 3$$

$$\text{throughput} = 247 \times \frac{2000}{[2000 + 6(3 + 1)]} = 244 \text{ MB / s}$$

The last option for /SYNC is a programmed /SYNC. This is the simplest option, which involves simply writing a '1' to the 'Send SYNC' bit of the FPDP_FLGS register. On the receive side, this value will arrive in the 'SYNC Received' bit of the FPDP_FLGS register.

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APPENDIX D

SL100/SL240 PROTOCOL

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D.1 Introduction



NOTE: The FibreXtreme SL100 and SL240 PCI, PMC, and CPCI Cards will be referred to throughout this appendix as PCI. Anything that is exclusive to the PCI, PMC, or CPCI Cards will be described as such.

The SL100/SL240 protocol (also known as VITA 17.1) is designed to provide near optimal throughput while maintaining low overhead. The link transfer rate for SL100 cards is 1.0625 Gbps, and the transfer rate for SL240 cards is 2.5 Gbps. Since an 8B/10B encoding scheme is used, this corresponds to a raw data rate of 106.25 MB/s (1 MB = 10^6 bytes) for SL100 and 250 MB/s for SL240. Based on the protocol presented here, the usable throughput of this link available to the user is 105 MB/s for SL100 or 247 MB/s for SL240. All ordered sets used by this protocol are standard Fibre Channel ordered sets with the exception of positive IDLE, which is allowed for a more flexible receiver interface.



NOTE: The protocol referred to throughout this document is the protocol used by the transmitter and accepted by the receiver. The receiver does not have to see the protocol defined here to receive data. Any generic Fibre Channel data stream with an IDLE at least every 4096 words can be used.

D.2 Ordered Sets Used

Fibre Channel denotes a certain mapping of the transmission words in the 8B/10B protocol to be ordered sets, which denote special control information for Fibre Channel. These same ordered sets are used in VITA 17.1, but are assigned different meaning.

There are eighteen ordered sets used by SL240 to denote different information. Twelve of these ordered sets are used to embed five bits of data - eight start-of-frame (SOF) sets are used to embed three bits at the start of a frame, and four status end-of-frame (SEOF) sets are used to embed two bits at the end of the frame. The SOF ordered sets embed three FPDP signals - PIO1, PIO2, and DIR.

Note that although the direction signal on FPDP is active low (/DIR), the signal transmitted on the link is active high (DIR).

The four EOF ordered sets embed the FPDP signal NRDY (once again, the inverted version of the FPDP interface's /NRDY) and transmit FIFO overflow flag.

There are two additional EOF ordered sets used by SL240 to denote the actual end of frame. The Mark EOF (MEOF) denotes a frame that has SYNC associated with it, and the Frame EOF (FEOF) denotes a normal data frame. The other four ordered sets are inter-frame padding used to denote flow control information and alternate frame interpretations. Table D-1 shows the mappings from the Fibre Channel ordered sets onto the VITA 17.1 ordered sets, along with the meaning associated with each ordered set.

Table D-1 Ordered Set Mapping

Fibre Channel Ordered Set	VITA 17.1 Ordered Set	Description
SOFc1	SOF	Start of Frame: PIO1 = 0, PIO2 = 0, DIR = 0
SOFi1	SOF	Start of Frame: PIO1 = 0, PIO2 = 0, DIR = 1
SOFn1	SOF	Start of Frame: PIO1 = 0, PIO2 = 1, DIR = 0
SOFi2	SOF	Start of Frame: PIO1 = 0, PIO2 = 1, DIR = 1
SOFn2	SOF	Start of Frame: PIO1 = 1, PIO2 = 0, DIR = 0
SOFi3	SOF	Start of Frame: PIO1 = 1, PIO2 = 0, DIR = 1
SOFn3	SOF	Start of Frame: PIO1 = 1, PIO2 = 1, DIR = 0
SOFf	SOF	Start of Frame: PIO1 = 1, PIO2 = 1, DIR = 1
EOFt	SEOF	Status EOF: FIFO Overflow = 0, NRDY = 0
EOFdt	SEOF	Status EOF: FIFO Overflow = 0, NRDY = 1
EOFa	SEOF	Status EOF: FIFO Overflow = 1, NRDY = 0
EOFn	SEOF	Status EOF: FIFO Overflow = 1, NRDY = 1
EOFni	MEOF	Mark EOF: EOF for a SYNC frame
EOFdti	FEOF	Frame EOF: EOF for a normal data frame
R_RDY	SWDV	SYNC with DATA Valid: Says that the next frame will be a SYNC with DATA frame
NOS	STOP	Tells the remote transmitter to stop sending data
CLS	GO	Tells the remote transmitter it can continue to send data
IDLE	IDLE	IDLE character: Used as a padding word to maintain receiver synchronization

D.3 Frames

There are three basic frame types defined in VITA 17.1—a data frame, a SYNC without data frame, and a SYNC with data frame. The data is divided into frames so the FPDP signals are sampled at some minimum interval, and so the receiver is guaranteed to see IDLEs to maintain synchronization. SYNC is used to delimit data streams and maintain host program synchronization. This signal is under user control for PCI based products, and is the same as the FPDP /SYNC signal for CMC/FPDP based products. The SL240 PCI cards will only generate SYNC frames as SYNC without DVALID frames.

Whenever a SYNC appears on the output of the transmit FIFO, the current frame is terminated and the proper SYNC frame (SYNC with data or SYNC without data) is sent. Figure D-1 shows the three types of frames and the ordered set placement within those frames.

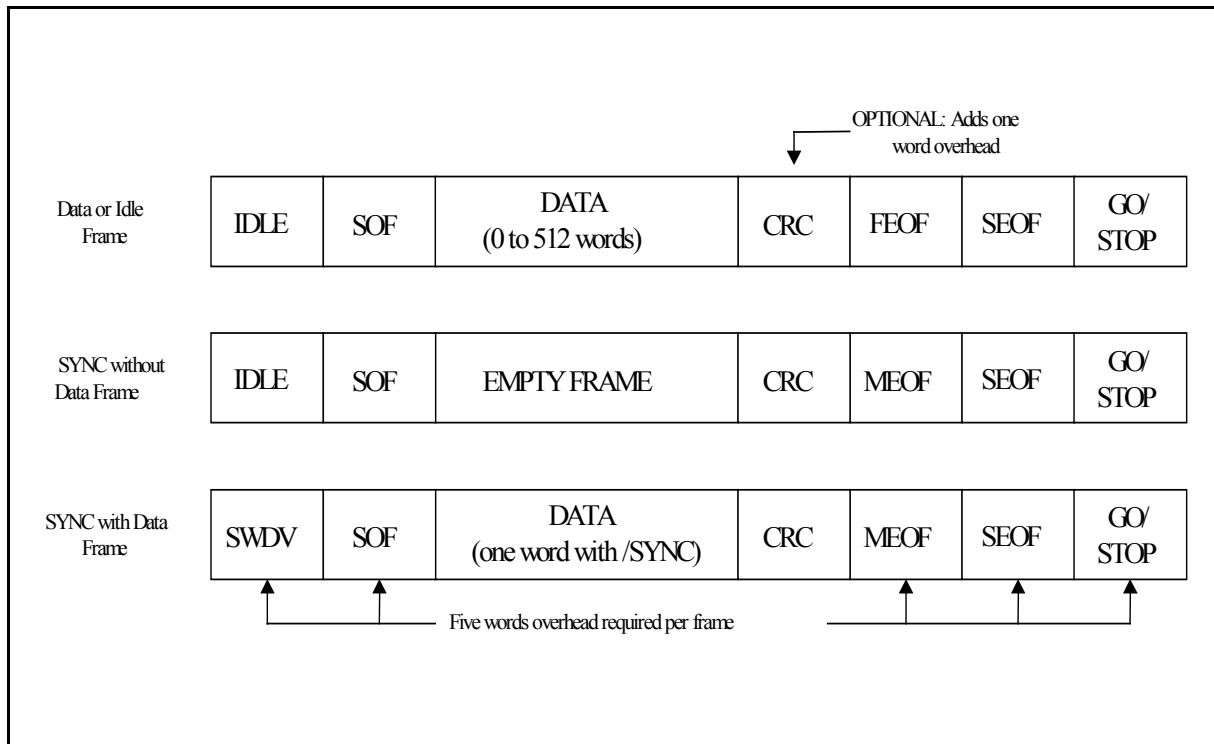


Figure D-1 VITA 17.1 Framing Protocol

D.3.1 Link Bandwidth

With CRC disabled, there is a five-word overhead for every frame transmitted. Since frames can contain up to 512 words of data, this results in an efficiency of 99.03%. With CRC enabled, there is a six-word overhead for every frame transmitted. This results in a maximum efficiency of 98.84%. Table D-2 gives the theoretical maximum sustained throughput based on these numbers.

Table D-2 Maximum Sustained Throughput

Card	With CRC	Without CRC
SL100	105.02 MB/s	105.22 MB/s
SL240	247.10 MB/s	247.58 MB/s

D.3.2 FPDP Signal Sample Rate

The states of the FPDP signals (PIO1, PIO2, DIR, and NRDY) are transmitted across the link at varying rates. The worst-case rate at which these signals are sampled is for CRC checked filled data frames. In this case, the signals are sampled every 518 words. Table D-3 summarizes the worst-case sampling frequencies for the different link transmission speeds (SL100 and SL240).

Table D-3 Sampling Frequencies

Card	With CRC	Without CRC
SL100	51.28 kHz	51.38 kHz
SL240	120.65 kHz	120.89 kHz

D.4 Data Transmission and Flow Control

As SL240 is seen as a point-to-point link from the transmitter, there is no need to log into the receiver node to begin sending data. SL240 boards can begin transmission as soon as they are started and data is available in the transmit FIFO. Using the frames described above, the transmitter sets up a constant stream of frames, into which it inserts data as it becomes available. Data is only inserted if the flow control signal from the remote end is GO—if it is STOP, then the data waits in the transmit FIFO until the signal changes. Systran's SL240 boards use the same protocol when transmitting from either end to allow the link to operate bi-directionally. Since these data streams are independent, the maximum throughput on the link would be 210 MB/s (105 MB/s/direction) for SL100 or 494 MB/s for SL240.

The receiver should transmit the STOP signal when it has space for the data contained in 20 km of fiber or less left. Assuming 5 μ s/km for the speed of light, this gives us 100 μ s of data. For SL100, each 32-bit word (40 bits on the link) takes 37.64 ns, there are 2657 words stored in 20 km of cable. For SL240, each 32-bit word (40 bits on the link) takes 16 ns, so there are 6250 words stored in 20 km of cable. The first 10 km is reserved for sending the STOP signal to the transmitter, and the second 10 km is for the data already contained in the receive fiber.

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APPENDIX E

ORDERING INFORMATION

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E.1 Overview

This appendix contains the order number for all Systran products mentioned in this manual. For an up to date list, or for inquiries about these products, contact Systran Sales.

E.2 Ordering Information

E.2.1 SL100 PMC Ordering Information

Order Number	Description
FHG4-PM4MWB04-00	SL100 PMC, 850 nm laser, 5 V PCI signaling voltage
FHG4-PM4SWB04-00	SL100 PMC, 1300 nm laser, 5 V PCI signaling voltage
FHG5-PM4MWB04-00	SL100 PMC, 850 nm laser, 3.3 V PCI signaling voltage
FHG5-PM4SWB04-00	SL100 PMC, 1300 nm laser, 3.3 V PCI signaling voltage
FHG4-PM4HSB04-00	SL100 PMC, HSSDC, 5 V PCI signaling voltage
FHG5-PM4HSB04-00	SL100 PMC, HSSDC, 3.3 V PCI signaling voltage
FHG4-PM4MWB04-R1	Ruggedized SL100 PMC, 850 nm laser, 5 V PCI signaling voltage
FHG5-PM4MWB04-R1	Ruggedized SL100 PMC, 850 nm laser, 3.3 V PCI signaling voltage
FHG4-PM4HSB04-R1	Ruggedized SL100 PMC, HSSDC, 5 V PCI signaling voltage
FHG5-PM4HSB04-R1	Ruggedized SL100 PMC, HSSDC, 3.3 V PCI signaling voltage

E.2.2 SL100 PCI Ordering Information

Order Number	Description
FHG4-PC4MWB04-00	SL100 PCI, 850 nm laser, 5 V PCI signaling voltage
FHG4-PC4SWB04-00	SL100 PCI, 1300 nm laser, 5 V PCI signaling voltage
FHG5-PC4MWB04-00	SL100 PCI, 850 nm laser, 3.3 V PCI signaling voltage
FHG5-PC4SWB04-00	SL100 PCI, 1300 nm laser, 3.3 V PCI signaling voltage
FHG4-PC4HSB04-00	SL100 PCI, HSSDC, 5 V PCI signaling voltage
FHG5-PC4HSB04-00	SL100 PCI, HSSDC, 3.3 V PCI signaling voltage

E.2.3 SL100 CPCI Ordering Information

Order Number	Description
FHG4-CP4MWB04-00	SL100 CPCI, 850 nm laser, 5 V PCI signaling voltage
FHG4-CP4SWB04-00	SL100 CPCI, 1300 nm laser, 5 V PCI signaling voltage
FHG5-CP4MWB04-00	SL100 CPCI, 850 nm laser, 3.3 V PCI signaling voltage
FHG5-CP4SWB04-00	SL100 CPCI, 1300 nm laser, 3.3 V PCI signaling voltage

E.2.4 SL100 FPDP Ordering Information

Order Number	Description
FHG4-FP4MWB04-00	NGSL VME with one FPDP port, SL100 CMC, 850 nm laser
FHG4-FP4SWB04-00	NGSL VME with one FPDP port, SL100 CMC, 1300 nm laser
FHG4-FM4MWB04-00	SL100 CMC, 850 nm laser
FHG4-FM4SWB04-00	SL100 CMC, 1300 nm laser
FHG4-FM4MWB04-R1	Ruggedized SL100 CMC, 850 nm laser
FHG2-FR4MWB04-00	Modified Single FXSL VME with two FPDP ports, SL100 CMC, 850 nm laser
FHG2-FR4SWB04-00	Modified Single FXSL VME with two FPDP ports, SL100 CMC, 1300 nm laser
FHG4-FSMWBMWB-00	Dual FXSL VME with two SL100 CMC cards, one FPDP port per CMC card, 850 nm laser
FHG4-FSSWBSWB-00	Dual FXSL VME with two SL100 CMC cards, one FPDP port per CMC card, 1300 nm laser

E.2.5 SL240 PMC Ordering Information

Order Number	Description
FHG6-PM6MWB04-00	SL240 PMC, 850 nm laser, 5 V PCI signaling voltage
FHG6-PM6SWB04-00	SL240 PMC, 1300 nm laser, 5 V PCI signaling voltage
FHG7-PM6MWB04-00	SL240 PMC, 850 nm laser, 3.3 V PCI signaling voltage
FHG7-PM6SWB04-00	SL240 PMC, 1300 nm laser, 3.3 V PCI signaling voltage

E.2.6 SL240 PCI Ordering Information

Order Number	Description
FHG6-PC6MWB04-00	SL240 PCI, 850 nm laser, 5 V PCI signaling voltage
FHG6-PC6SWB04-00	SL240 PCI, 1300 nm laser, 5 V PCI signaling voltage
FHG7-PC6MWB04-00	SL240 PCI, 850 nm laser, 3.3 V PCI signaling voltage
FHG7-PC6SWB04-00	SL240 PCI, 1300 nm laser, 3.3 V PCI signaling voltage

E.2.7 SL240 CPCI Ordering Information

Order Number	Description
FHG6-CP6MWB04-00	SL240 CPCI, 850 nm laser, 5 V PCI signaling voltage
FHG6-CP6SWB04-00	SL240 CPCI, 1300 nm laser, 5 V PCI signaling voltage
FHG7-CP6MWB04-00	SL240 CPCI, 850 nm laser, 3.3 V PCI signaling voltage
FHG7-CP6SWB04-00	SL240 CPCI, 1300 nm laser, 3.3 V PCI signaling voltage

E.2.8 SL240 FPDP Ordering Information

Order Number	Description
FHG6-FP6MWB04-00	NGSL VME with one FPDP port, SL240 CMC, 850 nm laser
FHG6-FP6SWB04-00	NGSL VME with one FPDP port, SL240 CMC, 1300 nm laser
FHG6-FM6MWB04-00	SL240 CMC, 850 nm laser
FHG6-FM6SWB04-00	SL240 CMC, 1300 nm laser
FHG6-FSMWBMWB-00	Dual FXSL VME with two SL240 CMC cards, one FPDP port per CMC card, 850 nm laser
FHG6-FSSWBSWB-00	Dual FXSL VME with two SL240 CMC cards, one FPDP port per CMC card, 1300 nm laser

E.2.9 VME Carrier

Order Number	Description
FHG4-FP000000-00	NGSL VME Carrier with one FPDP port (w/o CMC card)
FHG2-FP000000-00	Single FXSL Carrier with two FPDP Ports (w/o CMC card)
FHG2-FR000000-00	Modified Single FXSL Carrier with two FPDP Ports (w/o CMC card)

E.2.10 Multi-mode Fiber Optic Cables

All multi-mode fiber-optic cables are 50/125 μ m duplex cables.

Part Number	Length	Cable End 1	Cable End 2
FHAC-M2LC3000-00	3 meters	LC	LC
FHAC-M2LC5000-00	5 meters	LC	LC
FHAC-M2LC1001-00	10 meters	LC	LC
FHAC-M2LC2001-00	20 meters	LC	LC
FHAC-M2LC3001-00	30 meters	LC	LC
FHAC-M2LCxxxx-00	Custom	LC	LC

Part Number	Length	Cable End 1	Cable End 2
FHAC-M2LCST03-00	3 meters	LC	ST
FHAC-M2LCST05-00	5 meters	LC	ST
FHAC-M2LCST10-00	10 meters	LC	ST
FHAC-M2LCST20-00	20 meters	LC	ST
FHAC-M2LCST30-00	30 meters	LC	ST

Part Number	Length	Cable End 1	Cable End 2
FHAC-M2SCLC01-00	1 meter	SC	LC
FHAC-M2SCLC03-00	3 meters	SC	LC
FHAC-M2SCLC05-00	5 meters	SC	LC
FHAC-M2SCLC10-00	10 meters	SC	LC
FHAC-M2SCLC20-00	20 meters	SC	LC
FHAC-M2SCLC30-00	30 meters	SC	LC

E.2.11 Single-mode Fiber Optic Cables

All single-mode fiber-optic cables are 9/125 μ m duplex cables.

Part Number	Length	Cable End 1	Cable End 2
FHAC-S2LC3000-00	3 meters	LC	LC
FHAC-S2LC5000-00	5 meters	LC	LC
FHAC-S2LC1001-00	10 meters	LC	LC
FHAC-S2LC2001-00	20 meters	LC	LC
FHAC-S2LC3001-00	30 meters	LC	LC
FHAC-S2LCxxxx-00	Custom	LC	LC

Part Number	Length	Cable End 1	Cable End 2
FHAC-S2SCLC01-00	1 meter	SC	LC
FHAC-S2SCLC03-00	3 meters	SC	LC
FHAC-S2SCLC05-00	5 meters	SC	LC
FHAC-S2SCLC10-00	10 meters	SC	LC
FHAC-S2SCLC20-00	20 meters	SC	LC
FHAC-S2SCLC30-00	30 meters	SC	LC

E.2.12 HSSDC Copper: 150 Ω Shielded Quad Cable

Duplex, shielded quad cable with HSSDC connectors, for use with the HSSDC copper media interface.

Order Number	Description
FHAC-Q2HS1000-00	1 m duplex cable, equalized
FHAC-Q2HS3000-00	3 m duplex cable, equalized
FHAC-Q2HS5000-00	5 m duplex cable, equalized
FHAC-Q2HS1001-00	10 m duplex cable, equalized
FHAC-Q2HS2001-00	20 m duplex cable, equalized
FHAC-Q2HS2501-00	25 m duplex cable, equalized
FHAC-Q2HS3001-00	30 m duplex cable, equalized
FHAC-Q2H95000-00	5 m duplex cable, HSSDC to 9-pin D-sub

APPENDIX F

FPDP PRIMER

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F.1 FPDP Overview

This section provides a brief discussion of Front Panel Data Port (FPDP). For more information about FPDP, refer to *Front Panel Data Port Specifications, ANSI/VITA 17-1998* or go to the VITA website at: www.vita.com/vso/. The SL100/SL240 cards implement a serial version of FPDP on their link interface, which is standard VITA 17.1. Most of the concepts from the parallel FPDP specification are applicable to the serial FPDP world, so they are described here.

Many real-time systems require high-speed, low-latency data transfers on a sustained basis. However, the primary bus (for example, VME bus) cannot provide the required bandwidth and latency at all times because of bus contention. The primary bus must also handle other tasks such as system control. The FPDP bus provides a solution to this problem. Using FPDP, two or more cards are connected by a simple, parallel, synchronous interface using 80-conductor ribbon cable running across the cards' front panels or through a 1.0625 Gbps or 2.5 Gbps serial interface. For parallel FPDP, devices on the FPDP bus must consist of one FPDP Transmit Master (FPDP-TM) and one FPDP Receive Master (FPDP-RM). Multiple FPDP Receiver (FPDP-R) devices may also exist on the bus. For serial FPDP, there is one master for the bus (which acts as FPDP-TM and FPDP-RM), and one or more receiver nodes. Since only one FPDP-TM can exist on the bus, no bus contention between devices is possible. Figure F-1 shows an example VME FPDP card interconnection using parallel FPDP.

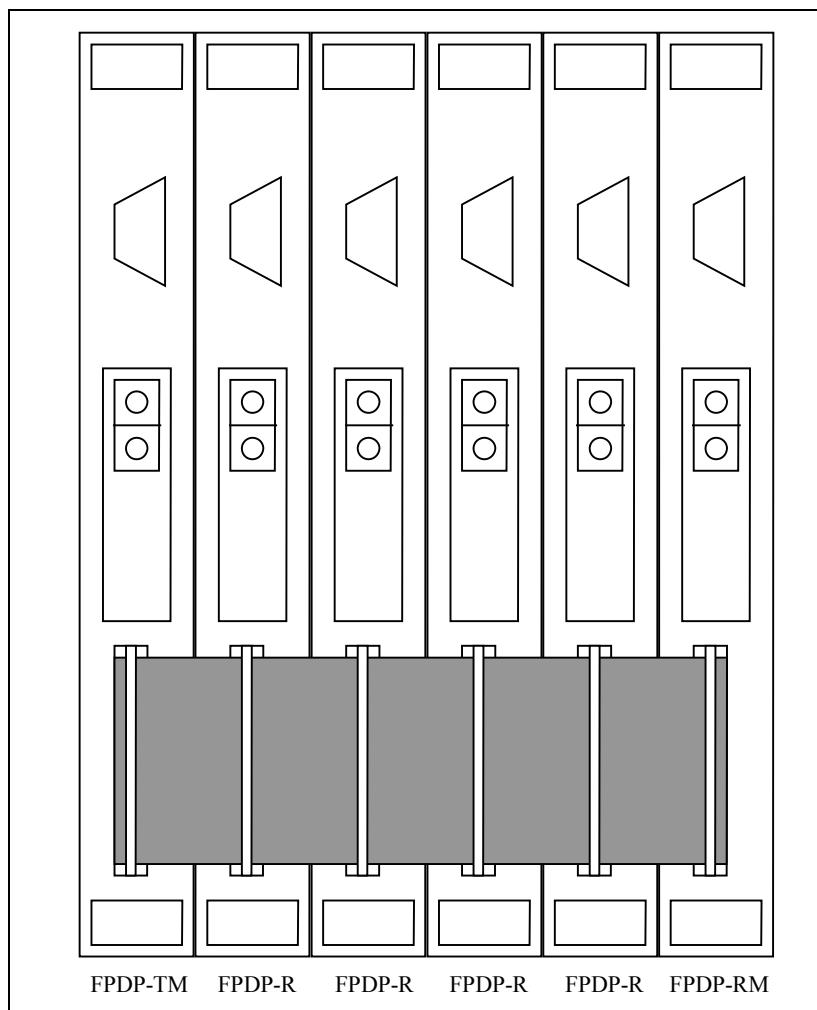


Figure F-1 Example Configuration With Multiple VME FPDP Cards Connected

Several advantages of an FPDP interface include:

- Simple hardware is required to interface to FPDP.
- FPDP does not interfere with the normal bus operations—VME or PCI traffic can continue without data transfers wasting bus bandwidth.
- No bus contention is possible because there is only one transmitter.
- No special backplane is required.
- FPDP allows connections from VME chassis to VME chassis.
- Systems may have multiple FPDP buses and thus provides scaleable bandwidth.
- Multiple FPDP busses may coexist in one chassis.
- Throughput can be accurately computed in the design stage.
- Little software development is required to move data between cards.
- Framed or unframed data may be transmitted across the FPDP link.
- Low latency.

Some additional advantages of parallel FPDP are:

- Low cost, 32-bit parallel interface provided through a ribbon cable.
- 160 MBps sustained data rate.

Some additional advantages of serial FPDP are:

- Noise immune fiber optic interface.
- Significantly increased transmission distance (10 km).
- Standard cards for parallel FPDP, custom backplanes, PCI (PCI/CPCI/PMC), and others available.

F.2 Terminology

Some FPDP specific terms are defined below.

FPDP TRANSMIT MASTER (FPDP-TM)

An FPDP-TM is a device that transmits data and timing signals onto the FPDP bus. This device also terminates the bus signals at one end of the ribbon cable bus for parallel FPDP. Only one FPDP-TM may exist on an FPDP bus. For serial FPDP, this device is the same as the FPDP-RM.

FPDP RECEIVE MASTER (FPDP-RM)

An FPDP-RM is a device that receives data from the FPDP bus synchronously with the timing signals provided by the FPDP-TM. This device also terminates the bus signals at one end of the ribbon cable bus for parallel FPDP. Only one FPDP-RM may exist on an FPDP bus. For serial FPDP, this device is the same as the FPDP-TM.

FPDP RECEIVER (FPDP-R)

An FPDP-R is a device that receives data from the FPDP bus synchronously with the timing signals provided by the FPDP-TM. As opposed to the FPDP-RM, this device does not terminate any bus signals on parallel FPDP. Multiple FPDP-R devices may exist on an FPDP bus. For serial FPDP, there are generally one or more FPDP-R devices on the bus.

F.3 Parallel FPDP Theory of Operation

F.3.1 Clock Signals

A single FPDP-TM generates a free-running clock. This clock frequency determines the maximum transfer rate on the bus. FPDP provides both a PECL (Positive Emitter Coupled Logic) and TTL strobe on the bus, with the PECL clock used for higher frequency (> 20 MHz) transfers. If designing to the CMC card, only an LVTTTL clock is generated by the card's FPDP transmitter port, since it is driving to a PCB instead of a long ribbon cable.

An FPDP receiver card (FPDP-R or FPDP-RM) accepts the PECL or TTL clock generated by the transmitter and uses it as the word clock for the data transfers. This clock is generally in the range of 0 to 40 MHz on standard FPDP busses, though the FPDP specification does not state a hard maximum frequency at which the bus may be run. The CMC card has a LVTTTL clock input that it uses for the word clock.

F.3.2 Data Framing

The FPDP specification does not allow for the transmission of address information. However, many systems have data coming from several cards or channels. The way to identify data from each channel is through framing. A synchronization pulse signal, /SYNC, was defined for framing purposes. The frame size is defined as the number of data items in the frame. Unframed data may also be transmitted onto the FPDP bus. The four data frame types defined by the FPDP specification are listed and described below.

- Unframed data
- Single frame data
- Fixed size repeating frame data
- Dynamic size repeating frame data

UNFRAMED DATA

- Used when the source and the organization of the data is not important.
- Used when the FPDP receivers do not need to be synchronized to the data stream.
- /SYNC is not required.

When unframed data is transmitted onto the FPDP bus, no synchronization is required. Thus, the FPDP-TM must not generate /SYNC, and the FPDP-RM and FPDP-R devices must not require a /SYNC pulse in order to correctly receive data.

SINGLE FRAME DATA

- Synchronization must occur prior to data to which it applies.
- Synchronization occurs between data blocks.
- /SYNC must be asserted before /DVALID is asserted.
- Synchronization occurs infrequently, perhaps only once.

When single frame data is transmitted onto the FPDP bus, the FPDP-TM must assert a /SYNC pulse before valid data starts being transmitted. Valid data is transmitted when the data valid signal /DVALID is asserted. Thus, a /SYNC pulse must be asserted before /DVALID is asserted when transmitting single frame data. After a /SYNC pulse is asserted, the FPDP-RM and FPDP-R devices should not accept data until the first STROBE period after /DVALID is asserted. The /SYNC pulse does not have to be asserted again until before the start of the next data transmission.

FIXED SIZE REPEATING FRAME DATA

- Synchronization must occur prior to data to which it applies.
- Synchronization occurs at the same time the last data word in the block before is transferred.
- /SYNC must be asserted at the end of the data block while /DVALID is still asserted.
- Because synchronization occurs at the end of the data block, the first data block will not be synchronized.
- Synchronization occurs frequently.
- All data frames are the same size.

When fixed or dynamic size repeating frame data is transmitted onto the FPDP bus, the FPDP-TM must assert a /SYNC pulse while /DVALID is already asserted. The /SYNC pulse must be asserted at the same time as the last data item of every frame. The FPDP-RM and FPDP-R devices must recognize that the current data is the last data item in current frame when both /SYNC and /DVALID are asserted. Since /SYNC is asserted at the end of a frame, the first data frame transmitted will not be synchronized. As a result, the system designer may wish to discard this first unsynchronized data frame. All data frames are the same size when fixed size repeating frame data is transmitted.

DYNAMIC SIZE REPEATING FRAME DATA

- Synchronization must occur prior to data to which it applies.
- Synchronization occurs at the same time the last data word in the block before is transferred.
- /SYNC must be asserted at the end of the data block while /DVALID is still asserted.
- Because synchronization occurs at the end of the data block, the first data block will not be synchronized.
- Synchronization occurs frequently.
- Data frames may vary in size.

For dynamic size repeating frame data, the behavior of the /SYNC pulse is the same as for fixed size repeating frame data, with the exception of varying sized frames.

F.4 Serial FPDP Theory of Operation

The protocol and framing for serial FPDP are listed in Appendix D. Serial FPDP operates similar to parallel FPDP with respect to maintaining data framing with the SYNC signal, but the SYNC signal does not correlate with data frames on the fiber. Any form of data framing listed in section F.3.2 can be mapped to serial FPDP, since the data stream and SYNCs are maintained. However, the timing may not be exactly the same as the parallel FPDP version due to link framing overhead and the fact that the link operates asynchronously to the parallel FPDP frequencies.

F.5 Parallel FPDP Signal Timing

Figure F-2 shows the timing for several FPDP interface signals. This figure is accurate for all four data framing types. See section F.3.2 for a discussion of framing. The Data Valid signal, /DVALID, is asserted by the FPDP-TM when valid data is transmitted onto the FPDP bus but not before at least 16 STROBE periods have occurred. The FPDP-TM must de-assert /DVALID when no more data remains in its buffer until valid data is again available. To avoid losing data when the receiver's FIFO is almost full, the receiver (FPDP-RM or FPDP-R) must assert the /SUSPEND signal to hold off the transmitter. The FPDP-TM must de-assert /DVALID within 16 STROBE periods and keep it de-asserted until /SUSPEND is de-asserted. Per the FPDP specification, after /SUSPEND is de-asserted, the FPDP-TM must wait for at least one STROBE period before re-asserting /DVALID. With the FibreXtreme SL240 card, after /SUSPEND is de-asserted, the FPDP-TM must wait for at least two STROBE periods before re-asserting /DVALID. The /SUSPEND signal is asynchronous to the STROBE clock and should be double synchronized by the FPDP-TM before being used in order to avoid metastability problems.

The FPDP-TM must not transmit data onto the FPDP bus until the Not Ready signal, /NRDY, is de-asserted by the FPDP-RM and FPDP-R devices. The FPDP-RM and FPDP-R devices must assert /NRDY when they are not ready to accept data and must de-assert /NRDY otherwise. The /NRDY signal is asynchronous to the STROBE clock and should be double synchronized by the FPDP-TM before being used in order to avoid metastability problems.

As required by the *Front Panel Data Port Specifications, ANSI/VITA 17-1998*, the FPDP-TM transmits the Data Direction signal /DIR. The /DIR signal must be asserted at least 16 STROBE periods before /DVALID is asserted. FPDP-RM and FPDP-R devices may receive /DIR. The /DIR signal is not given a firm definition of use. Possible uses of this signal include providing a status indication available to be read by software or to allow operation to be inhibited until /DIR is asserted. The /DIR signal may be asynchronous with other FPDP signals. With the SL240 FPDP card, the FPDP-TM asserts /DIR, waits 16 STROBE periods, and then starts transmitting data onto the FPDP bus. This is the only way that the SL240 FPDP card currently uses this signal.

Two user-defined Programmable I/O (PIO) signals, PIO1 and PIO2, are reserved in the *Front Panel Data Port Specifications*. These are auxiliary signals that are not required for core FPDP functions. However, these signals can be user-defined to allow the FPDP-TM, FPDP-RM, and FPDP-R devices to transfer information that is not part of the FPDP specifications. The FPDP-TM, FPDP-RM, and FPDP-R devices must not drive either of the PIO lines immediately at power up of the system. This is to avoid the possibility of two devices driving the same PIO line simultaneously and causing damage to the driver device.

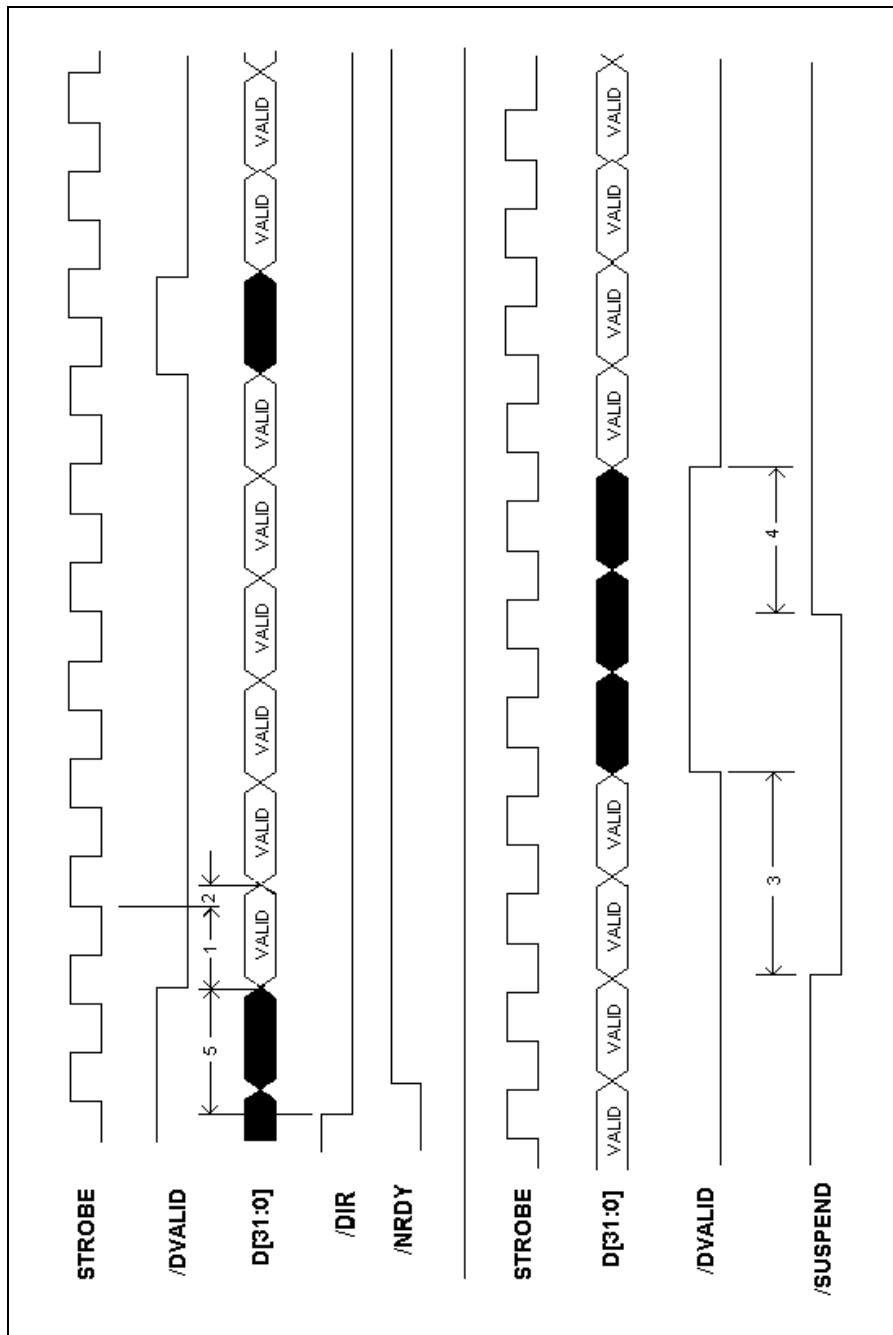


Figure F-2 Parallel FPDP Interface Timing Diagram

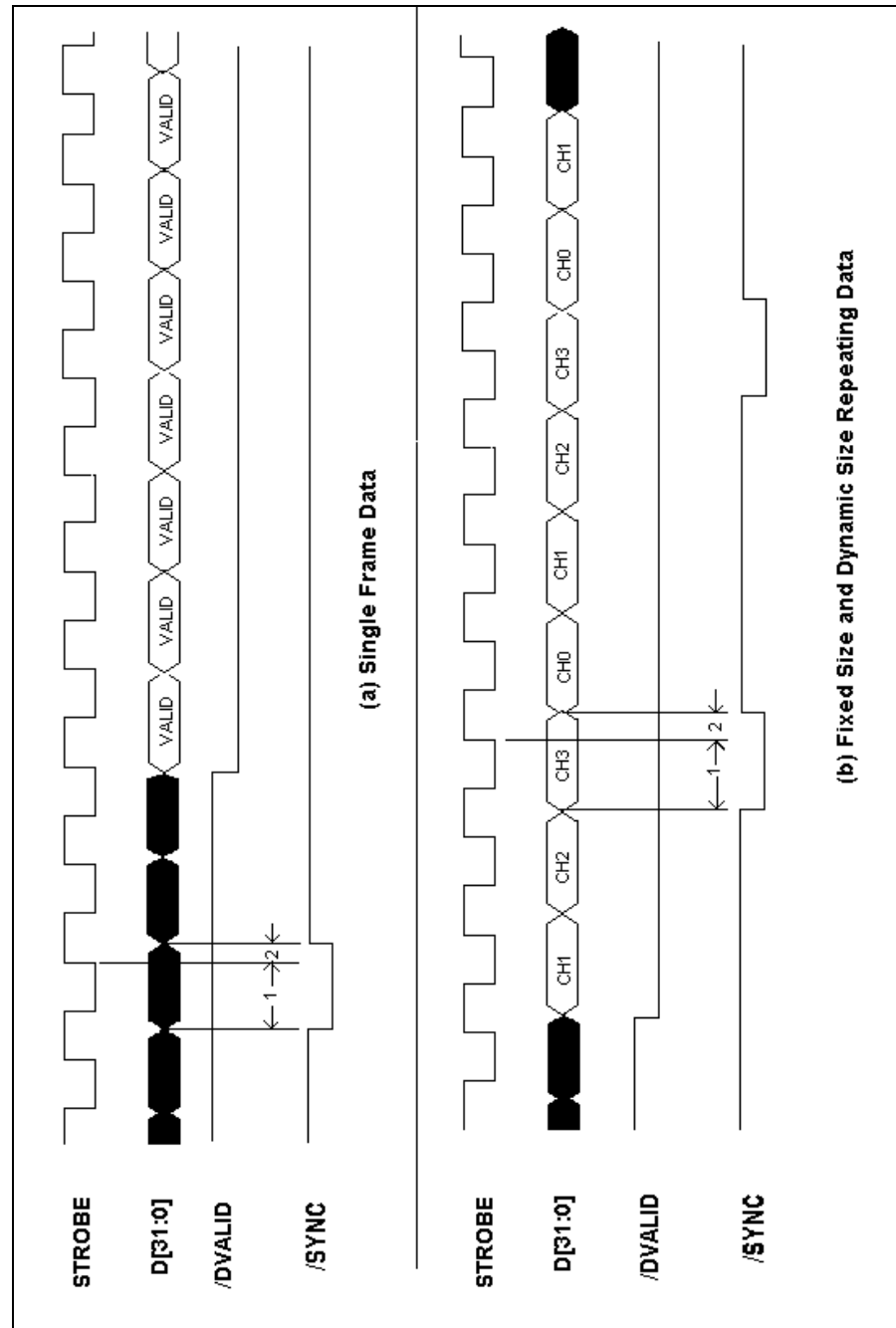


Figure F-3 FPDP Timing Diagrams Showing the Use of Framing

The timing parameters from Figure F-2 and Figure F-3 are detailed in Table F-1 for the transmitter interface.

Table F-1 Transmitter Interface Timing Parameters

Parameter	Description	Min	Max
1	Data, /DVALID , /SYNC setup time	10 ns	---
2	Data, /DVALID , /SYNC hold time	0 ns	---
3	/SUSPEND asserted to data stop	---	16 clocks
4	/SUSPEND de-asserted to data started	1 clock	---
5	/DIR asserted to /DVALID asserted	16 clocks	---

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GLOSSARY

1x3 -----	A 3-pin connector for use with copper media.
8B/10B -----	A data encoding scheme developed by IBM for translating byte-wide data to an encoded 10-bit format.
AAL5 -----	ATM Adaptation Layer for computer data.
active -----	A term used to denote a port that is receiving a signal.
AL -----	Arbitrated Loop. Fibre Channel topology where L_Ports use arbitration to establish a point-to-point circuit without hubs or switches.
ALPA -----	Arbitrated Loop Physical Address.
ANSI -----	American National Standards Institute.
AP -----	Access Point.
API -----	Applications Program Interface.
APID -----	Access Point Identification Number. A number ranging between 0 and 65535 that is assigned by the user to identify a process. All APID's attached to a single FX board must be unique.
ASIC -----	Application Specific Integrated Circuit. An integrated circuit designed to perform a specific function. ASICs are typically made up of several interconnected building blocks and can be quite large and complex.
ATM -----	Asynchronous Transfer Mode. A network technology which transfers data in small 53-byte packets and permits transmission over long distances. Proposed speeds range from 25 Mbps to 622 Mbps.
bandwidth -----	The amount of data that can be transmitted over a channel.
baud -----	A unit of speed in data transmission, usually equal to one bit per second.
Bi-Directional card -----	A FibreXtreme Simplex Link card with both source and destination capabilities.
BIOS -----	Basic Input/Output System.
bps -----	bits per second.
broadcast -----	Sending a transmission to all nodes on a network.
BSP -----	Board Support Package. A set of software routines written by the OS vendor or SBC vendor which provide support for a particular SBC.
burst transfers -----	Messages are transmitted in a format that includes the initial address followed by all the data. Burst transfers eliminate the need for repeated addresses for each data block, permitting higher throughput.
channel -----	A point-to-point link that transports data from one point to another at the highest speed with the least delay, performing simple error correction in hardware. Channels are hardware intensive and have lower overhead than networks. Channels do not have the burden of station management.
channel network -----	Combines the best attributes of both channel and network, giving high bandwidth, low latency I/O for client server. Performance is measured in transactions per second instead of packets per second.
circuit -----	Bi-directional path allowing communications between two L_Ports.

circuit-switched mode	-----	Data transfer through a dedicated connection (Class 1).
CMC	-----	Common Mezzanine Card.
communications protocol	----	A special sequence of control characters that are exchanged between a computer and a remote terminal in order to establish synchronous communication.
CRC	-----	Cyclic Redundancy Check. A code used to check for errors in Fibre Channel.
datagram	-----	Type of data transfer for Class 3 service. Transfer has no confirmation of receipt and rapid data transmission.
dBm	-----	decibels relative to one milliwatt.
destination only card	-----	A FibreXtreme Simplex Link card that is only capable of receiving data.
direct connect links	-----	An actual physical, dedicated connection between two devices with the entire bandwidth available to serve each direct link. Direct links provide a fast and reliable medium for sending large volumes of data.
DMA	-----	Direct Memory Access.
DMA write	-----	The DMA engine on the bus controller writes the data from the host computer to the SRAM buffer, freeing the host CPU for other tasks. (FibreXpress board becomes a master for the bus.)
E_Port	-----	Element Port. Used to connect fabric elements together.
ECL	-----	Emitter Coupled Logic.
ethernet	-----	A widely used shared networking technology.
exchange	-----	One or more sequences for a single operation that are not concurrent, but are grouped together.
F_Port	-----	Fabric Port. The access point of the fabric for physically connecting the user's N_Port.
fabric	-----	A self-managed, active, intelligent switching mechanism that handles routing in Fibre Channel Networks.
fabric elements	-----	Another name for ports.
FC	-----	Fibre Channel.
FC-AL	-----	Fibre Channel Arbitrated Loop. Provides a low-cost way to attach multiple ports in a loop without hubs and switches.
FCP	-----	Fibre Channel Protocol. The mapping of the SCSI communication protocol over Fibre Channel.
FC-PH	-----	Fibre Channel Physical interface. Fibre Channel Physical standard, consisting of the three lower levels, FC-0, FC-1, and FC-2.
FCSI	-----	Fibre Channel Systems Initiative is made up of IBM, Hewlett-Packard and Sun Microsystems. This group strives to advance Fibre Channel as an affordable, high-speed interconnection standard.
FC-SW	-----	Fibre Channel Switch Fabric standard. Formerly known as FC-XS: Fibre Channel Xpoint Switch. The crosspoint-switched fabric topology is the

	highest-performance Fibre Channel fabric, providing a choice of multiple path routings between pairs of F_ports.
Fibre Channel -----	Fibre Channel (FC) is a serial data transfer interface technology operating at speeds up to 1 Gbps. It is defined as an open standard by ANSI. It operates over copper and fiber optic cabling at distances of up to 10 kilometers. Supported topologies include point-to-point, arbitrated-loop, and fabric switches.
FibreXpress -----	A Systran trademark name for the Fibre Channel family of products.
FibreXtreme -----	A Systran trademark name for the Simplex Link family of products.
FibreXtreme Simplex Link ---	A high-speed, point-to-point, communication network capable of transfers in excess of 100 MB/s.
FIFO -----	first in first out
Firmware -----	Microprocessor executable code, typically for embedded type processors.
Flash -----	A type of Electrical Erasable Programmable Read Only Memory (EEPROM). Erased and written to in blocks vs. bytes.
FL_Port -----	Fabric Loop Port. Joins an arbitrated loop to the fabric.
FPDP -----	Front Panel Data Port.
frame -----	A linear set of transmitted bits that define a basic transport element. A frame is the smallest indivisible packet of data that is sent on the FC.
frame-switched mode -----	Data transfer is connectionless (Classes 2 and 3) and data transmission is in frames. The bandwidth is allocated on a link-by-link basis. Frames from same port are independently switched and may take different paths.
FTP application -----	A test application for transferring files from one computer to another.
FX -----	FibreXpress.
G_Port -----	A port which can function as either an F_Port or an E_Port. Its function is defined at login.
Gbps -----	Gigabits per second.
gigabit -----	One billion bits, or one thousand megabits.
GLM -----	Gigabit per second Link Module. A Link Module that can be used for optical or copper media.
HANDLE -----	Abstraction for the <i>Handle</i> in Windows and <i>file descriptor</i> in Unix.
HBA -----	Host Bus Adapter.
HIPPI -----	High Performance Parallel Interface. An 800 Mbps interface to supercomputer networks (previously called high-speed channel) developed by ANSI.
HSSDC -----	High Speed Serial Data Connectors and Cable Assemblies. A type of high-speed interconnect system which allows for transmission of data rates greater than 2 Gbps and up to 30 meters.

hunt group -----	A group of lines that are linked so that one call to the group will find the line that is free. This provides the ability for more than one port to respond to the same alias address.
I/O -----	Input/Output.
IOCB -----	I/O Control Block. A block of information stored in system memory, usually of fixed length, which contains control codes and data. The IOCB is created by a host computer and sent to some other computer. The IOCB contains command/instructions, data, and memory pointers intended to direct the other computer to perform some function.
inactive -----	A term used to denote a port that is not receiving a signal.
intermix -----	A Fibre-Channel-defined mode of service that reserves the full Fibre Channel bandwidth for a dedicated (Class 1) connection, but also allows connectionless (Class 2) traffic to share the link if the bandwidth is available.
IP -----	Internet Protocol is a data communications protocol.
IPI -----	Intelligent Peripheral Interface.
insertion delay -----	The amount of time the data is delayed for the insertion of FXSL framing protocol. It is measured from when the data becomes available at the FIFO to when the data is actually transmitted on the link. The actual values are either 188 ns in Mode-0 or Mode-1 (with no CRC), or 226 ns in Mode-2 or Mode-3 (with CRC).
kB -----	KiloBytes.
L_Port -----	Loop Port. Either an FL_Port or an NL_Port that supports the arbitrated loop topology.
LAN -----	Local Area Network, typically less than 5 kilometers. Transmissions within a LAN are mostly digital, carrying data at rates above 1 Mbps.
latency -----	The delay between the initiation of data transmission and the receipt of data at its destination.
LCF -----	Link_Control Facility. Provides logical interface between nodes and the rest of Fibre Channel.
Link Module -----	A mezzanine board mounted on the board to interface between the board and the network.
longword -----	32-bit or 4-byte word.
LP -----	Lightweight Protocol.
LX1500 -----	LinkXchange LX1500 Crossbar Switch.
LX2500 -----	LinkXchange LX2500 Crossbar Switch.
Mbps -----	Megabits per second.
MBps -----	MegaBytes per second.
MB -----	MegaBytes.

media -----	Means of connecting nodes; either fibre optics, coaxial cable or unshielded twisted pair.
monitor -----	An application program used to display the status and change the configuration of the driver.
multicast -----	A single transmission is sent to multiple destination N_ports.
N_Port -----	Node Port. A Fibre-Channel-defined entity at the node end of a link that connects to the fabric via an F-Port.
network -----	Connects a group of nodes, providing the protocol that supports interaction among these nodes. Networks are software intensive, and have high overhead. Networks also operate in an environment of unanticipated connections. Networks have a limited ability to provide the I/O bandwidth required by today's applications and client/server architectures.
NL_Port -----	Node Loop Port. Joins nodes on an arbitrated loop.
node -----	A host computer and interface board. Each processor, disk array, work station or any computing device is called a node. Connects to FC through a node port (N_Port).
normal write -----	A host CPU writes data to the SRAM buffer through the bus and bus controller (FibreXpress board operates as a slave of the bus).
ns -----	nanoseconds.
NVRAM -----	Non-Volatile Random Access Memory. Generic term for memory that retains its contents when power is turned off.
OFC -----	Open Fibre Control. A safety interlock system used on some FC shortwave links.
operation -----	One of Fibre Channel's building blocks composed of one or more exchanges.
out-of-band control -----	On the LinkXchange products, a method of issuing switch commands that does not use any bandwidth of the 32 switch ports.
PCI -----	Peripheral Component Interface.
PIO -----	Programmed Input/Output.
PMC -----	PCI Mezzanine Card. Everything that is true for PCI cards is true for PMC except there is a footprint or card format change.
port -----	A physical element through which information passes. It is an electrical or optical interface with a pair of wires or fibers—one each for incoming and outgoing data.
profiles -----	Subsets of Fibre Channel standards that improve interoperability and simplify implementation. It is like a cross-section of FC, providing guidelines for implementing a particular application.

protocols -----	Data transmission conventions encompassing timing, control, formatting, and data representation. This set of hardware and software interfaces in a terminal or computer allow it to transmit over a communication network, and these conventions collectively form a communications language.
RISC -----	Reduced Instruction Set Computer. A type of microprocessor that executes a limited number of instructions that typically allows it to run faster than a Complex Instruction Set Computer (CISC).
SAP -----	Service Access Point.
SBC -----	Single Board Computer.
SCSI -----	Small Computer System Interface.
sequence -----	The unit of transfer, made up of one or more related frames for a single operation.
shared connect links -----	The ability to send and receive data without establishing a dedicated physical connection so that other devices can also use the medium. This shared link is more efficient for smaller data transmissions because the overhead of direct connect link is avoided.
SRAM -----	Static Random Access Memory.
SRAM Transfer -----	Process in which the data is transferred from the host computer to the SRAM buffer by normal or by DMA write.
STP -----	Shielded Twisted Pair. A type of cable media.
striping -----	To multiply bandwidth by using multiple ports in parallel.
switched fabric -----	(see the definition for “fabric”).
SYNC -----	FibreXtreme Simplex Link primitive used to synchronize the source and destination cards.
SYNC with dvalid -----	A special case of the SYNC primitive occurring in the middle of a buffer of data.
source only card -----	A FibreXtreme Simplex Link card that is only capable of sending data.
TCP -----	Transmission Control Protocol.
terminal application -----	A test application that sends characters received from the keyboard and displays received characters.
throughput application -----	An application that tests the throughput for the given system.
time-out -----	The time allotted for a native message to travel the network ring and return. If this time is exceeded, an automatic retransmission of the native message occurs.
topology -----	Refers to the order of information flow due to logical and physical arrangement of stations on a network.
ULP -----	Upper Level Protocol.
VHDL -----	Very high-speed integrated circuit Hardware Description Language.
VME -----	Acronym for VERSA-module Europe: a bus architecture used in some computers.

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