FILAR

Quad HOLA S-LINK to 64-bit/66 MHz PCI Interface

Users Guide

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Revision History

Date	Author	Modification
2 May 2002	EB	First version
17 May 2002	EB	Changed page sizes. Explanation disabling temperature interrupt. REQFIFO W/O
27 May 2002	EB	Redone fig.1. Added MJ as author, Test Input Register and test bit in OPCTL

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FILAR

Introduction

The FILAR is a highly integrated PCI interface that can move data from up to four HOLA S-LINK channels to a 32-bit or 64-bit PCI bus that runs at 33 MHz or at 66 MHz. The interface can only be used in 3.3 Volt PCI slots.

Four HOLA Link Destinations are integrated on the FILAR. The channels are fully compatible to HOLA Link Source Cards and each can receive data at a speed of up to 160 MB/s. There are versions of the interface available in which not all channels are mounted. The Operation Status register will show which channels are not available.

For each channel, the host processor can set up the interface to receive up to fifteen S-LINK data blocks by writing the host memory addresses where the data has to be stored to the Request FIFO (figure 1). After this, the interface can receive data without needing any intervention of the processor. After reception of data, the host processor can read from the Acknowledge FIFO the S-LINK control words and the length of the data block received.

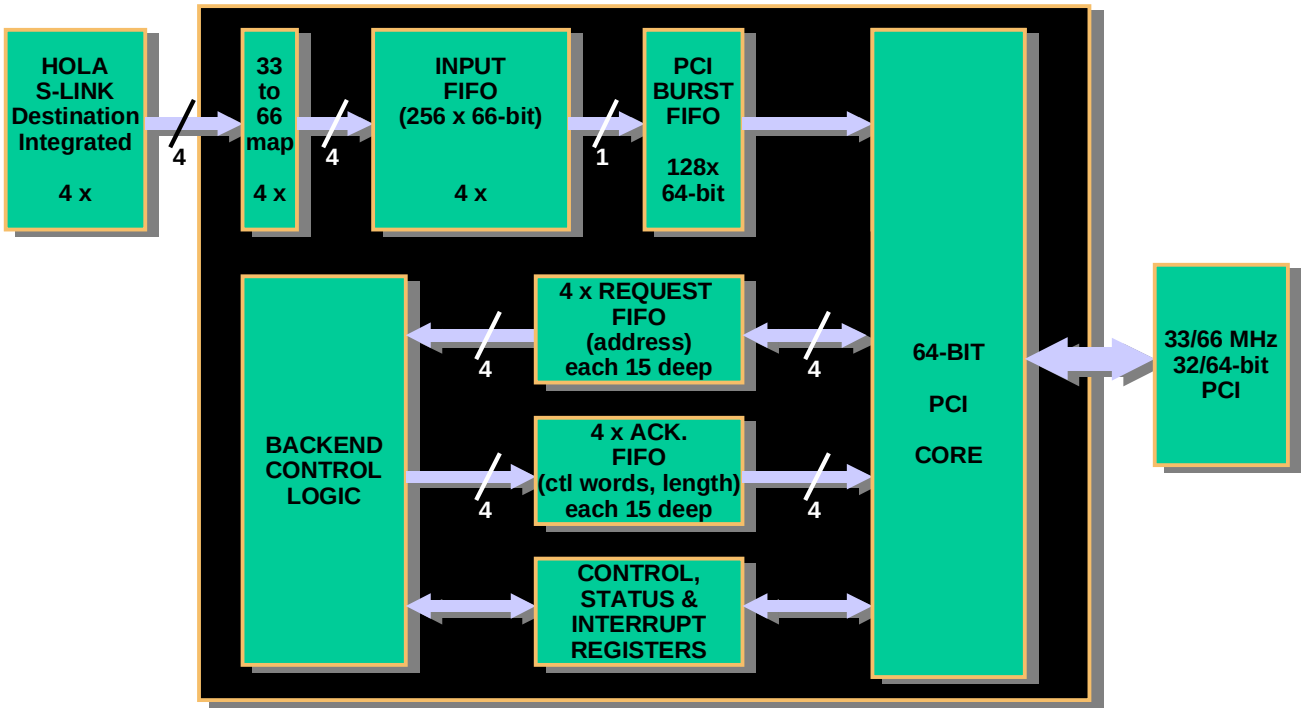

Figure 1: block diagram of the FILAR

Features

The main features of the interface are:

- highly autonomous data reception
- reception speed independent of interrupt or polling latency
- interrupt generation selectable on reception of one or several data blocks, link down, space available in Request FIFO and others.
- control words stored independently from data
- control words checked for known values, improving overhead
- programmable word and byte swapping of data words
- four integrated optical HOLA Destination input links
- throughput of each input link up to 160 MB/s
- card temperature readout
- 32-bit and 64-bit PCI bus (3.3V PCI bus only)
- 33 and 66 MHz MHz PCI clock speed
- 32-bit PCI-bus addressing

PCI Configuration registers

The PCI configuration registers are the standard registers that every PCI compatible card has. Detailed information on the usage of those registers can be found in the PCI Specification

Vendor Identification Register (VID)

Register name	Vendor Identification (VID)
Address offset	00-01h
Boot-load	10DCh (CERN)
Attribute	Read Only (RO)
Size	16 bits

Device Identification Register (DID)

Register name	Device Identification (DID)
Address offset	02-03h
Boot-load	0013h (FILAR, Quad ODIN S-LINK to 64-bit PCI interface)
Attribute	Read Only (RO)
Size	16 bits

PCI Command Register (PCICMD)

Register name	PCI Command (PCICMD)
Address offset	04-05h
Boot-load	0000h
Attribute	Read/Write (R/W on 6 bits, Read Only on all others)
Size	16 bits

PCI Status Register (PCISTS)

Register name	PCI Status (PCISTS)
Address offset	06-07h
Boot-load	0080h
Attribute	Read Only (RO), Read/Write Clear (R/WC)
Size	16 bits

Revision Identification Register (RID)

Register name	Revision Identification (RID)
Address offset	08h
Boot-load	00h (version 0.0 - 2 May 2002). Field will be updated with each version
Attribute	Read Only (RO)
Size	8 bits

Class Code Register (CLCD)

Register name	Class Code (CLCD)
Address offset	09-0Bh
Boot-load	028000h (network controller/other communication device/programming interface 00h)
Attribute	Read Only (RO)
Size	24 bits

Cache Line Size Register (CALN)

Register name	Cache Line Size
Address offset	0Ch
Boot-load	00h
Attribute	Read Only (RO)
Size	8 bits

Latency Timer Register (LAT)

Register name	Latency Timer (LAT)
Address offset	0Dh
Boot-load	FFh
Attribute	Read/Write (R/W)
Size	8 bits

Header Type Register (HDR)

Register name	Header Type (HDR)
Address offset	0Eh
Boot-load	00h (Single function, Format field 0)
Attribute	Read Only (RO)
Size	8 bits

Built-in Self-test Register (BIST)

Register name	Built-in Self-test (BIST)
Address offset	0Fh
Boot-load	00h
Attribute	D7, D5-0 Read Only, D6 as PCI bus write only
Size	8 bits

Base Address Register 0 (BADR0)

Register name	Base Address 0 (BADR0)
Address offset	10h
Boot-load	FFFFFC00h (1024 bytes in memory space)
Attribute	High bits Read/Write; low bits Read Only
Size	32 bits

Base Address Register 1-5 (BADR1-BADR5)

Register name	Base Address 1-5 (BADR1-BADR5)
Address offset	14h, 18h, 1Ch, 20h, 24h
Boot-load	00000000h (disabled)
Attribute	High bits Read/Write; low bits Read Only
Size	32 bits

CardBus CIS Pointer

Register name	CardBus CIS Pointer
Address offset	28h
Boot-load	00000000h
Attribute	Read Only
Size	32 bits

Subsystem Vendor ID

Register name	Subsystem Vendor ID
Address offset	2Ch
Boot-load	0000h
Attribute	Read Only
Size	16 bits

Subsystem Device ID

Register name	Subsystem Device ID
Address offset	2Eh
Boot-load	00h
Attribute	Read Only
Size	16 bits

Expansion ROM Base Address Register (XROM)

Register name	Expansion ROM Base Address (XROM)
Address offset	30h
Boot-load	00000000h (disabled)
Attribute	bits 31:11, bit 0 Read/Write; bits 10:1 Read Only
Size	32 bits

Capabilities Pointer

Register name	Capabilities Pointer
Address offset	34h
Boot-load	00h
Attribute	Read Only
Size	8 bits

Interrupt Line Register (INTLN)

Register name	Interrupt Line (INTLN)
Address offset	3Ch
Boot-load	FFh (unknown)
Attribute	Read/Write
Size	8 bits

Interrupt Pin Register (INTPIN)

Register name	Interrupt Pin (INTPIN)
Address offset	3Dh
Boot-load	01h (INTA#)
Attribute	Read Only (RO)
Size	8 bits

Minimum Grant Register (MINGNT)

Register name	Minimum Grant (MINGNT)
Address offset	3Eh
Boot-load	00h (no stringent requirement)
Attribute	Read Only (RO)
Size	8 bits

Maximum Latency Register (MAXLAT)

Register name	Maximum Latency (MAXLAT)
Address offset	3Fh
Boot-load	00h (no stringent requirement)
Attribute	Read Only (RO)
Size	8 bits

Operation Registers

Memory map

The operation registers are mapped into the PCI Memory Space. The base address can be found in Base Address Register 0 of the PCI Configuration Space. The interface occupies 1 KByte in Memory Space. There are no registers located in the PCI I/O Space.

You can access the registers with 32-bit PCI cycles only.

Register	Address offset
Operation Control	000h
Operation Status	004h
Interrupt Mask	008h
FIFO Status	00Ch
Start Control Word	010h
End Control Word	014h
Test Input	018h
reserved	01Ch-0FCh
Channel 1 Request FIFO	100h
Channel 1 Acknowledge FIFO	104h
reserved	108h
reserved	10Ch
Channel 2 Request FIFO	110h
Channel 2 Acknowledge FIFO	114h
reserved	118h
reserved	11Ch
Channel 3 Request FIFO	120h
Channel 3 Acknowledge FIFO	124h
reserved	128h
reserved	12Ch
Channel 4 Request FIFO	130h
Channel 4 Acknowledge FIFO	134h
reserved	138h
reserved	13Ch
reserved	140h-3FCh

Operation Control Register (OPCTL)

Register name	Operation Control register (OPCTL)
Address offset	000h
Boot-load	00000000h
Attribute	Read/Write
Size	32 bits

Bit 31-28	CH4 URL3-0 User Return Lines
Bit 27	CH4 DISABLE 0=normal operation 1=disable channel
Bit 26	CH4 URESET 0=normal operation 1=reset S-LINK See protocol with LDOWN#. This bit is inverted from the signal to the S-LINK.
Bit 25-22	CH3 URL3-0
Bit 21	CH3 DISABLE
Bit 20	CH3 URESET
Bit 19-16	CH2 URL3-0
Bit 15	CH2 DISABLE
Bit 14	CH2 URESET
Bit 13-10	CH1 URL3-0
Bit 9	CH1 DISABLE
Bit 8	CH1 URESET
Bit 7	reserved, write as 0, ignore on read
Bit 6	TSTMODE: testmode 0=normal operation 1=test mode In test mode data is taken from the Test Input register.
Bit 5-3	PAGE_SIZE [Bytes] 000 = 256 100 = 16384 001 = 1024 101 = 65536 010 = 2048 110 = 262144 011 = 4096 111 = 4194296
Bit 2	SWAP_WORD 0=no swap of 32-bit data words 1=swap of 32-bit data words E.g. 0xAABBCCDD_EEFF0011 becomes 0xEEFF0011_AABBCCDD
Bit 1	SWAP_BYTE 0=no byte swap of data words

	1=byte swap of all data words E.g. 0x11223344 becomes 0x44332211
Bit 0	RESET_IF 0=normal operation 1=reset interface

Description

The URL bits of this register are connected to the User Return Lines of the S-LINK interface and have the functionality as described in the S-LINK specification.

The DISABLE bits are used to disable individual channels. A channel may be disabled because a channel is not connected or if a channel is not presenting valid information. If the optical transceiver of a channel is not mounted, the FILAR will automatically disable that channel.

The URESET bits are used to reset the S-LINK interface. Note that the value in this bit has the inverted level of the URESET# signal to the S-LINK. To reset an S-LINK interface, the sequence as described in the S-LINK specification has to be followed with the LDOWN# signal. The status of LDOWN# can be read in the Operation Status Register.

The UTDO# lines of the S-LINK interfaces are fixed to 0, meaning that the FILAR will always receive test data when the link is put in test mode. Also the UDW (User DataWidth) lines are fixed to 0.

TSTMODE (bit 6) tells the interface to go into test mode. In this case the Test Input Register is used to feed data into the interface and data coming from the input links is discarded.

The PAGE_SIZE field (bits 5 to 3) sets the maximum amount of data that the FILAR will write to the host memory area that is pointed to by a Request FIFO entry. If more data is received than set by the PAGE_SIZE, a second Request FIFO entry will be used to store the remaining data. The PAGE_SIZE includes only the count of data words and does not include the control words. Note that the setting “111” gives a page size of 4 MByte-8 (and not exactly 4 MByte) which is the maximum length that can be shown by the 20-bit received length field (in words) in the Acknowledge FIFOs.

When bit 2 (SWAP_WORD) is set, the two 32-bit words in all received data words will be swapped. E.g. data received as 0xAABBCCDD_EEFF0011 becomes 0xEEFF0011_AABBCCDD. When set, the swap will be made only on data words. Control words will not be swapped. The swap mode used is the same for all channels.

When bit 1 (SWAP_BYTE) is set, the bytes in all received data words will be swapped so that words received in little endian format will be transformed into big endian or vice versa. E.g. the received word 0x11223344 becomes 0x44332211. When set, the swap will be made only on data words. Control words will not be swapped. The swap mode used is the same for all channels.

Bit 0, RESET_IF will reset the complete interface. It will reset all internal FIFOs, state machines and the DMA engine. After writing a 1 to this register, it may take up to one microsecond before the interface is operational again. To operate, the bit has to be reset to 0. To reset the interface it is possible to write a 1, immediately followed by a write of a 0. RESET_IF will not reset the HOLA S-LINK channels; they have to be reset separately with the URESET bits.

Operation Status Register (OPSTAT)

Register name	Operation Status register (OPSTAT)
Address offset	004h
Attribute	Read Only (RO)
Size	32 bits

Bit 31	CH4 NOT_PRESENT 0=normal operation of channel 1=channel logic not implemented or not connected
Bit 30	CH4 UXOFF 0=normal S-LINK activity 1=S-LINK transfer has been suspended since last read of the OPSTAT register. Note that this bit is inverted from the signal to the S-LINK. Bit is reset automatically after read of the OPSTAT register.
Bit 29	CH4 OVFLW 0=normal S-LINK activity 1=overflow occurred since last read of the OPSTAT register. Bit is reset automatic-ally after read of the OPSTAT register.
Bit 28	CH4 LDOWN 0=link is up 1=link is down Note that this bit is inverted from the signal to the S-LINK
Bit 27	CH3 NOT_PRESENT
Bit 26	CH3 UXOFF
Bit 25	CH3 OVFLW
Bit 24	CH3 LDOWN
Bit 23	CH2 NOT_PRESENT
Bit 22	CH2 UXOFF
Bit 21	CH2 OVFLW
Bit 20	CH2 LDOWN
Bit 19	CH1 NOT_PRESENT
Bit 18	CH1 UXOFF
Bit 17	CH1 OVFLW
Bit 16	CH1 URESET

Bit 15-8	TEMPERATURE Temperature of card in degrees C (0-255)
Bit 7-2	reserved, ignore value
Bit 1	ACK_AVAILABLE 0=no ACK_FIFO entries filled 1=at least one ACK_FIFO entry filled
Bit 0	REQ_AVAILABLE 0=no REQ_FIFO entries free 1=at least one REQ_FIFO entry free

Description

A FILAR may be delivered in a configuration in which not all channels are present. The NOT_PRESENT bits show for each channel if it is not functional because the optical transceiver or other logic is not mounted.

The UXOFF bit of each channel shows that the S-LINK flow control signal UXOFF# has been active since last read of the Operation Status Register. That is, the data transfer has been suspended for a period of time because the interface could not move the data fast enough out of its internal buffers to the main memory. E.g. the PCI bus was used by other masters, there were no outstanding REQ_FIFO entries or the ACK_FIFO was full. Once set, the bit will be reset automatically after the read of the Operation Status Register. There is no possibility to read the actual state of the UXOFF signal. When UXOFF has been active, it only means that the data transfer has temporary been interrupted, but no data will be lost because of this.

The OVFLW bit of each channel will be set when the internal input buffer FIFO is overflown. This is an error condition that may never happen as the S-LINK provides flow control. When an OVFLW bit is set, the interface will continue to work, but data may be lost. Once set, the bit will be reset automatically after the read of the Operation Status Register.

The LDOWN bit of each channel shows the current state of the S-LINK LDOWN# line. If the bit is 1, it means that the link is down. To get the link up again, a reset of the link is required. To reset an S-LINK interface, the protocol between the URESET# and LDOWN# signals as described in the S-LINK specification has to be followed.

The ACK_AVAILABLE bit shows if there is any Acknowledge FIFO entry available to be read. You must read the FIFO Status Register to find out which Acknowledge FIFO may be read from.

The REQ_AVAILABLE bits shows if there is any Request FIFO entry available to be written. You must read the FIFO Status Register to find out which Request FIFO may be written to.

Interrupt Mask Register (INTMASK)

Register name	Interrupt Mask register (INTMASK)
Address offset	008h
Boot-load	00000000h
Attribute	Read/Write
Size	32 bits

Bit 31	reserved, write as 0, ignore on read
Bit 30	CH4 UXOFF 1=interupt when UXOFF is 1
Bit 29	CH4 OVFLW 1=interrupt when FIFO is overflown
Bit 28	CH4 LDOWN 1=interrupt when link is down
Bit 27	reserved, write as 0, ignore on read
Bit 26	CH3 UXOFF
Bit 25	CH3 OVFLW
Bit 24	CH3 LDOWN
Bit 23	reserved, write as 0, ignore on read
Bit 22	CH2 UXOFF
Bit 21	CH2 OVFLW
Bit 20	CH2 LDOWN
Bit 19	reserved, write as 0, ignore on read
Bit 18	CH1 UXOFF
Bit 17	CH1 OVFLW
Bit 16	CH1 LDOWN
Bit 15-8	MAX_TEMP Interrupt when the temperature of the card is equal or above the value written in this field in degrees C (1-255). 0=disable interrupt on temperature

Bit 7-2	reserved, write as 0, ignore on read
Bit 1	ACK_AVAILABLE 1=interrupt when at least one ACK_FIFO entry is filled
Bit 0	REQ_AVAILABLE 1=interrupt when at least one REQ_FIFO entry is free

Description

The Interrupt Mask Register is used to enable interrupts on certain events in the Operation Status Register. If a bit in the Interrupt Mask is set to 1, and the corresponding bit in the Operation Status Register is set to 1, a PCI interrupt will be generated.

The interrupt will stay active until the reason for the it has been removed or that the interrupt is masked. The MAX_TEMP interrupt normally will be deactivated by masking the it.

FIFO Status Register (FSTAT)

Register name	FIFO Status Register (FSTAT)
Address offset	00Ch
Attribute	Read Only
Size	32 bits

Bit 31-28	CH4 REQ_AVAILABLE Number of entries that can be written to the Request FIFO
Bit 27-24	CH4 ACK_AVAILABLE Number of entries that can be read from the Acknowledge FIFO
Bit 23-20	CH3 REQ_AVAILABLE
Bit 19-16	CH3 ACK_AVAILABLE
Bit 15-12	CH2 REQ_AVAILABLE
Bit 11-8	CH2 ACK_AVAILABLE
Bit 7-4	CH1 REQ_AVAILABLE
Bit 3-0	CH1 ACK_AVAILABLE

Description

The FIFO Status Register shows in a single register the status of the FIFOs of all four channels.

The REQ_AVAILABLE bits give a total count of the number of entries that may be written to the Request FIFO before it will be filled. E.g. if the number is three, up to three entries may be written.

The ACK_AVAILABLE bits give a total count of the number of entries that are available to read from the Acknowledge FIFO. E.g. if the number is three, up to three entries may be read.

Start Control Word Register (SCTL)

Register name	Start Control Word Register (SCTL)
Address offset	010h
Attribute	Read Only
Size	32 bits

Bit 31-0	Start Control Word

Description

The Start Control Word register gives the start control word that belongs to the last ACKFIFO entry read. It is a single register that is shared between the different channels. So if an Acknowledge FIFO entry of Channel 2 is read, this register will give the Start Control Word (if present) of the last entry read of Channel 2.

End Control Word Register (ECTL)

Register name	End Control Word Register (ECTL)
Address offset	014h
Attribute	Read Only
Size	32 bits

Bit 31-0	End Control Word

Description

The End Control Word register gives the end control word that belongs to the last ACKFIFO entry read. It is a single register that is shared between the different channels. So if an Acknowledge FIFO entry of Channel 2 is read, this register will give the End Control Word (if present) of the last entry read of Channel 2.

Test Input Register (TSTIN)

Register name	Test Input Register (TSTIN)
Address offset	018h
Attribute	Read/Write
Size	32 bits

Bit 31-5	reserved, write as 0, ignore on read
Bit 4	CH4 TST Write a word to channel 4
Bit 3	CH3 TST Write a word to channel 3
Bit 2	CH2 TST Write a word to channel 2
Bit 1	CH1 TST Write a word to channel 1
Bit 0	TSTCNTL 0=write as data word 1=write as control word

Description

This register is used for testing purposes only.

If enabled in the Operation Control Register by setting bit 6 (TSTMODE), a write to the TSTIN register will behave as if a single S-LINK word has been received. Bits 1 to 4 determine to which channel the data gets written; several bits may be set. Bit 0 (TSTCNTL) determines if the test word is received as an S-LINK control word or as a normal data word.

After a reset, the test data is 0x0000_0001. Every word written afterwards will be shifted and left rotated. I.e. the first word will be 0x0000_0001, the second one 0x0000_0002. After 0x8000_0000 it will start over with 0x000_0001.

Request FIFOs (REQFIFOx)

Register name	Request FIFO x (REQFIFOx)
Address offset	Channel 1: 100h Channel 2: 110h Channel 3: 120h Channel 4: 130h
Attribute	Write Only
Size	32 bits

Bit 31-0	START_ADDRESS Start Address. Must be on a 64-bit address boundary.

Description

The Request FIFOs are used to tell the interface where to store the data received from the S-LINK. Each channel has its own Request FIFO. The Start Address must be on a 64-bit address boundary, i.e. bits 2 to 0 must be set to 0.

When a channel receives data, it will store the received start control word in the Acknowledge FIFO and the data in the host memory starting from the Start Address. Data will be transferred to the host memory until either a second control word is received or that the Page Size as set in the Operation Control register is reached. If a second control word is received before the Page Size is reached, the control word and the length of the received block are put in the Acknowledge FIFO. If the Maximum Block Length is reached before receiving a control word, the data that follows will be put in the memory starting from the Start Address from the next Request FIFO entry.

Request FIFO entries are handled in the order that they are written to the FIFO. The interface will continue to receive data until all requests are handled or that the Acknowledge FIFO is full.

Before writing to the Request FIFO address, you should check the REQ_AVAILABLE field in the FIFO Status Register to verify that there is still space available or else requests may be lost. In total up to fifteen receive requests may be outstanding for each channel.

Acknowledge FIFOs (ACKFIFOx)

Register name	Acknowledge FIFO x (ACKFIFOx)
Address offset	Channel 1: 104h Channel 2: 114h Channel 3: 124h Channel 4: 134h
Attribute	Read Only
Size	32 bits

Bit 31	S_CNTL_ABSNT Start Control Word absent 0: Start control word present 1: Start control word absent. I.e. the transfer started without a control word. Ignore Start Control Word register and S_CNTL_WRONG bit.
Bit 30	S_CNTL_WRONG 0: Start Control Word is B0F0xxx0h 1: Start Control Word is not B0F0xxx0h
Bit 29	E_CNTL_ABSNT End Control Word not present 0: End control word present 1: End control word not absent. I.e. the Page Size as set in the Operation Control register was reached. Ignore End Control Word register and E_CNTL_WRONG bit.
Bit 28	E_CNTL_WRONG 0: End Control Word is E0F0xxx0h 1: End Control Word is not E0F0xxx0h
Bit 27-20	reserved, ignore value
Bit 19-0	RX_BLOCK_LENGTH Received Block Length in 32-bit words

Description

The interface writes to the Acknowledge FIFO whenever an S-LINK block of data is received. Each channel has its own Acknowledge FIFO.

Normally data is sent in between two control words:

Start control word
Data
End control word

The interface will store the control words that encapsulate the S-LINK data and the length of the received block in the Acknowledge FIFO. If the starting or ending control word is not present, it will be shown by bits 31 and 29 respectively. The actual data is stored in the host memory starting from the address as it was given by the first available entry in the Request

FIFO. Entries in the Request FIFO will be handled on a First In, First Out basis.

After the read of an Acknowledge FIFO entry, a read of the Start Control Word register (address offset 010h) will return the Start Control word, while a read of the End Control Word register (address offset 014h) will return the End Control word. If the S_CNTL_ABSNT or E_CNTL_ABSNT bits of an entry is 1, the Start Control Word register or End Control Word register contents should be ignored.

Received Start and End control words are checked against the values B0F0xxx0h and E0F0xxx0h respectively. The upper part (B0F0h and E0F0h) are values used in the ATLAS data acquisition system. The lowest 0h will check for the error detection field in the control word, as a 0h represents no error in the control word nor in the datablock received before the control word. In applications where the transmitter sends the given control words, there is no need to read the control words from the Start and End Control Word registers, so the overhead gets reduced. Only in case of errors the Control Word registers need to be read. Applications that use other values will always need to read the Start and End Control Word registers and will have a slightly larger overhead.

The received number of S-LINK words is counted in 32-bit word quantities. Although the maximum block length value in the Request FIFO must be an even number of 32-bit words, the interface can receive an odd number of 32-bit S-LINK words and will correctly show the number in the RX_BLOCK_LENGTH field. The Received Block Length field is 20 bits wide, but its value will never exceed the value as set by the PAGE_SIZE field in the Operation Control register.

The interface ignores the value of the LDERR# signal of S-LINK, which can be done as every type of S-LINK makes the error detection information also available in the two least significant bits of control words. For applications that would use S-LINK data words only and no control words, there is no possibility to receive link error detection information. Therefore the use of data formats without control words is strongly discouraged.

The following examples show the contents of the Acknowledge FIFO for five possible cases: the block of data received is smaller, the same size, up to twice the size, exactly twice the size and more than twice the size of MAX_BLOCK_LENGTH that was set in the Request FIFO.

In the cases that the size of a block is exactly the same as requested in the Request FIFO or a multiple of it, the end control word will be put in a separate Acknowledge FIFO entry with the RX_BLOCK_LENGTH set to 0. The reason for this is that the interface will already fill the Acknowledge FIFO when the requested amount of data is received. It will not wait for the end control word. In fact those cases are similar to the ones where the amount of received data did not fit in a single entry, but just with zero extra data words received. Therefore the driver software should not have to consider those as special cases.

Example 1: reception of a 1000 32-bit words packet encapsulated in between control words, with PAGE_SIZE set to 1024.

S_CNTL_ABSNT	0 (start control word present)
E_CNTL_ABSNT	0 (end control word present)
RX_BLOCK_LENGTH	1000

Example 2: reception of a 1024 32-bit words packet encapsulated in between control words, with PAGE_SIZE set to 1024. In this case two Request FIFO entries are used.

S_CNTL_ABSNT	0 (start control word present)
E_CNTL_ABSNT	1 (end control word absent)
RX_BLOCK_LENGTH	1024
S_CNTL_ABSNT	1 (start control word absent)
E_CNTL_ABSNT	0 (end control word present)
RX_BLOCK_LENGTH	0

Example 3: reception of a 2000 32-bit words packet encapsulated in between control words, with PAGE_SIZE set to 1024.

S_CNTL_ABSNT	0 (start control word present)
E_CNTL_ABSNT	1 (end control word absent)
RX_BLOCK_LENGTH	1024
S_CNTL_ABSNT	1 (start control word absent)
E_CNTL_ABSNT	0 (end control word present)
RX_BLOCK_LENGTH	976

Example 4: reception of a 2048 32-bit words packet encapsulated in between control words, with PAGE_SIZE set to 1024. In this case three Request FIFO entries are used

S_CNTL_ABSNT	0 (start control word present)
E_CNTL_ABSNT	1 (end control word absent)
RX_BLOCK_LENGTH	1024
S_CNTL_ABSNT	1 (start control word absent)
E_CNTL_ABSNT	1 (end control word absent)
RX_BLOCK_LENGTH	1024
S_CNTL_ABSNT	1 (start control word absent)
E_CNTL_ABSNT	0 (end control word present)
RX_BLOCK_LENGTH	0

Example 5: reception of a 2100 32-bit words packet encapsulated in between control words, with PAGE_SIZE set to 1024.

S_CNTL_ABSNT	0 (start control word present)
E_CNTL_ABSNT	1 (end control word absent)
RX_BLOCK_LENGTH	1024
S_CNTL_ABSNT	1 (start control word absent)
E_CNTL_ABSNT	1 (end control word absent)
RX_BLOCK_LENGTH	1024
S_CNTL_ABSNT	1 (start control word absent)
E_CNTL_ABSNT	0 (end control word present)
RX_BLOCK_LENGTH	52