A photograph of a lush green forest with a flowing stream. The water flows over mossy rocks, creating white foam. Two small orange birds with black caps are standing on mossy rocks on the right side of the stream.

# MONSOON –Torrent

## Production Readiness Review

### Functional and Electrical Description 1

Peter Moore

# **Torrent Pedigree** from the MONSOON “*Functional and Performance Requirements*” Document - MNSN-AD-04-0001.

## System Purpose

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The MONSOON Image Acquisition System will be a scalable, multi-channel, high-speed image acquisition system. MONSOON must meet or exceed all of the needs of the currently defined, or anticipated in the next ten years, next generation NOAO systems requiring image acquisition capabilities regardless of wavelength or underlying detector technology.

It is fortunate that, the basic needs for these systems are constant regardless of detector technology.

- The need for an interface to the user with the ability for image acquisition parameter definition and image request.
- The need to interface to the technical staff for system configuration and system diagnostics.
- The need for interface to the telescope, instrument, and observatory to acquire status for FITS header information.
- The need to acquire “detector limited” images in an efficient manner which maximizes “open shutter” or integration time.
- The need to interface to the image handling system to pass the ~~packaged~~ FITS image off to the observatory system and observer.

See <http://www.noao.edu/ets/monsoon/techdoclist.html>



## Area of application

This self contained detector controller shall have sufficient functionality to replace actual detector controllers in use through the astronomical community without compromising existing performance.

## Advantage / motivation

Replace unreliable or high maintenance hardware.

Replace hardware that cannot be repaired because of obsolete components.

Unify detector controller architectures to reduce maintenance burden.

Applied to new instrumentation without risk of 'single source' components.

## Project lifecycle

| Project Phase    | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 |
|------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Development      |      | XX   | XXX  | XXX  |      |      |      |      |      |      |      |      |      |
| Evaluation       |      |      | XX   | XXX  | XX   |      |      |      |      |      |      |      |      |
| Production       |      |      |      | X    | XXX  | X    |      |      |      |      |      |      |      |
| Deployment       |      |      |      |      | XXX  | XXX  | X    |      |      |      |      |      |      |
| Enhancement      |      |      |      |      | XX   | XX   |      |      |      |      | X    |      |      |
| Operational Life |      |      |      |      | XX   | XXX  |
| Obsolescence     |      |      |      |      |      |      |      |      |      |      | ???? |      |      |

## Generic qualities

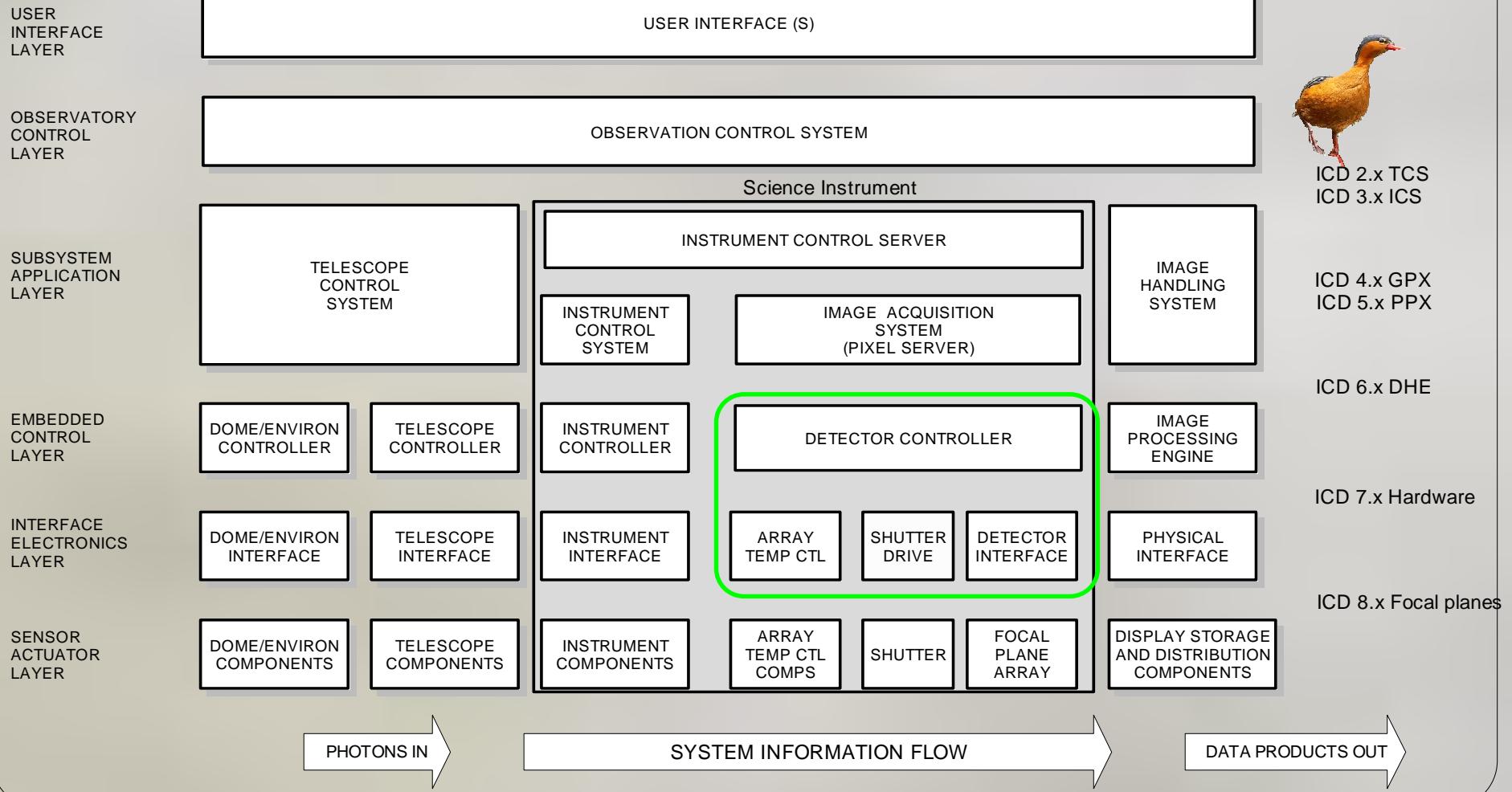
The application of the controller to specific functionality shall be through selection of a board suite, hardware configuration, and 'runtime' configuration options. The hardware assembly shall be called the Detector Head Electronics (DHE) package. Current plans for board suite selection for the DHE are:

- Generic Local Control Board.
- CCD Analog Front End board.
- IR Analog Front End board.
- Power supply board.
- Utility Board (Temperature control, Shutter).
- Preamp board (or Current Source board for IR).

The cost to purchase shall be consistent to the required capabilities i.e. cost should scale with number of video channels, etc. Baseline cost for a four channel CCD system is \$10k

- The controller hardware will be compatible with existing Pixel Acquisition Node (PAN) hardware and software.
- Support for card serial numbers, auto-configuration, and auto-calibration using expanded NOAO software suite, support for comprehensive telemetry sensing, support for card temperature sensing.

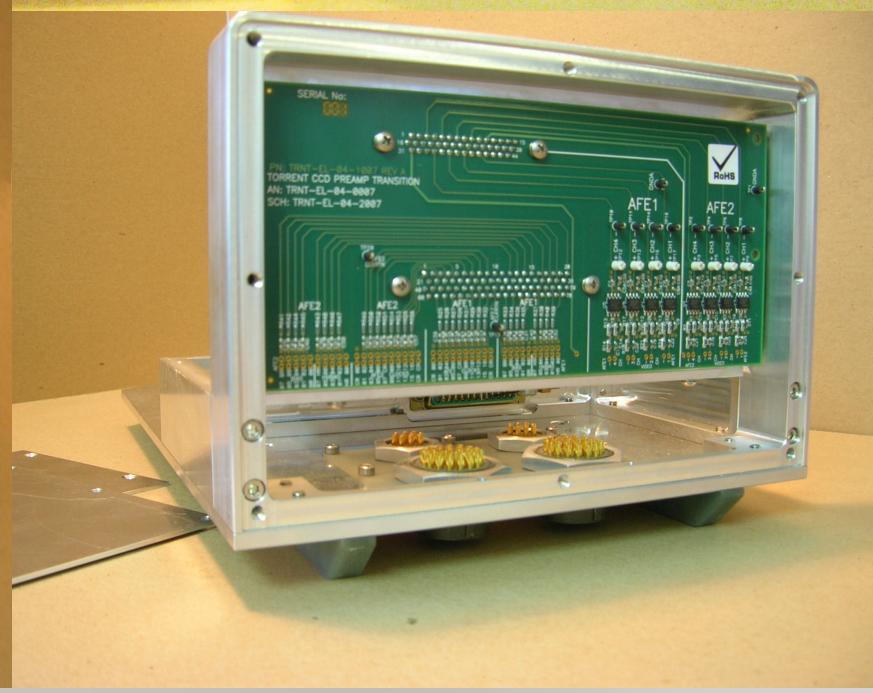
## OBSERVATORY SYSTEM REFERENCE MODEL



See <http://www.noao.edu/ets/monsoon/ICD.html>

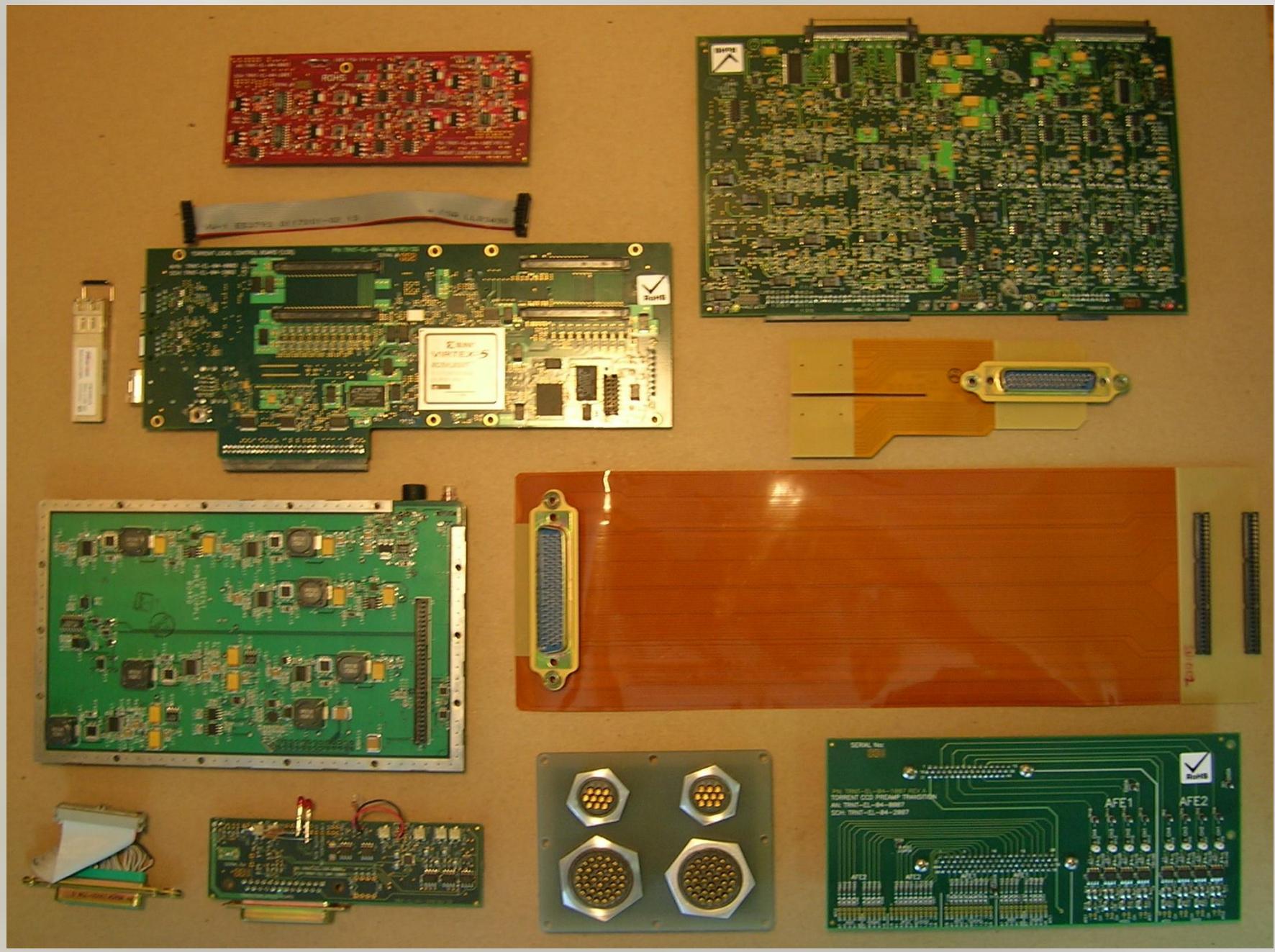
# Torrent Design – DHE Survival and Access

6



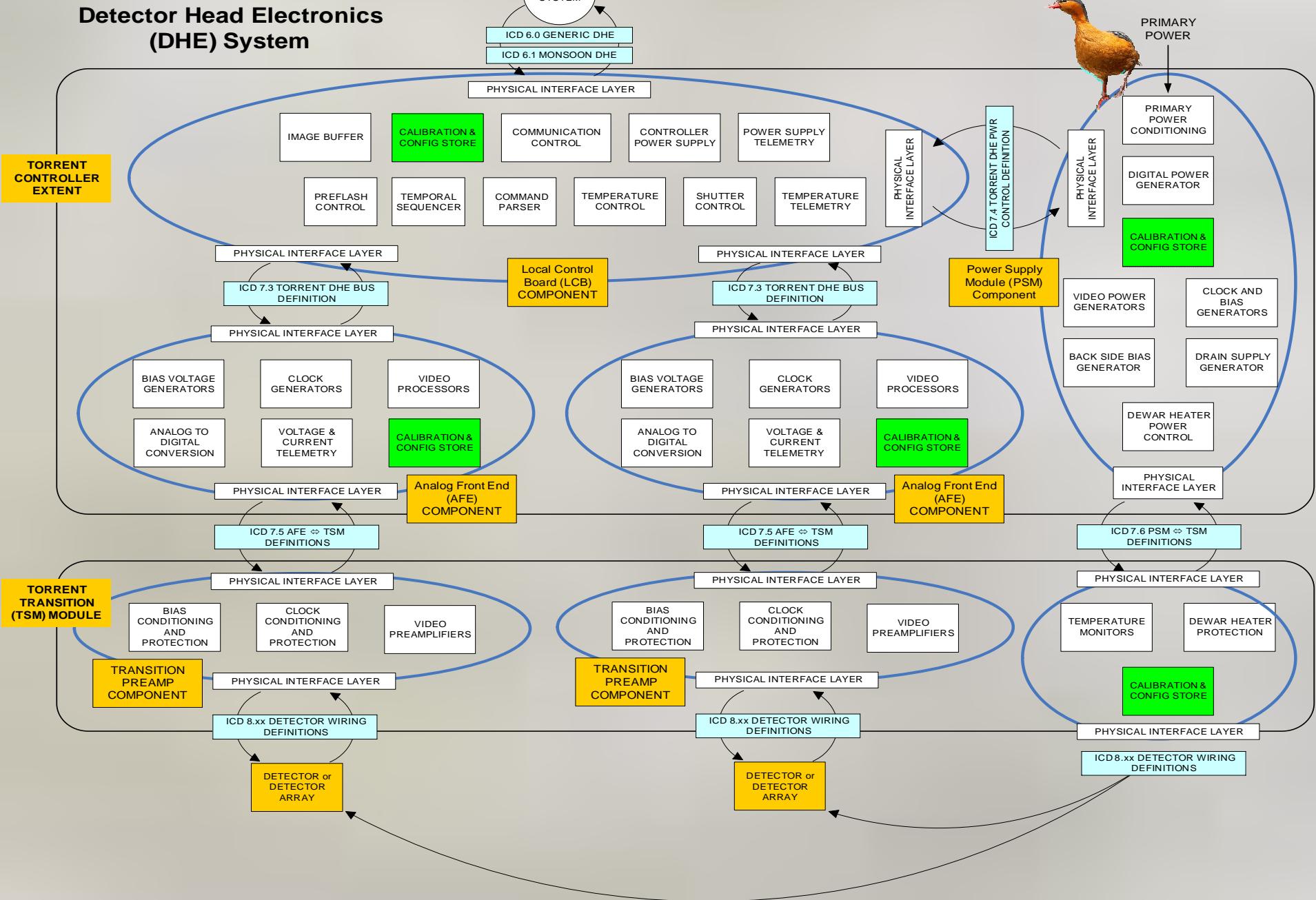
# Torrent Design – DHE Hardware Board Set

7

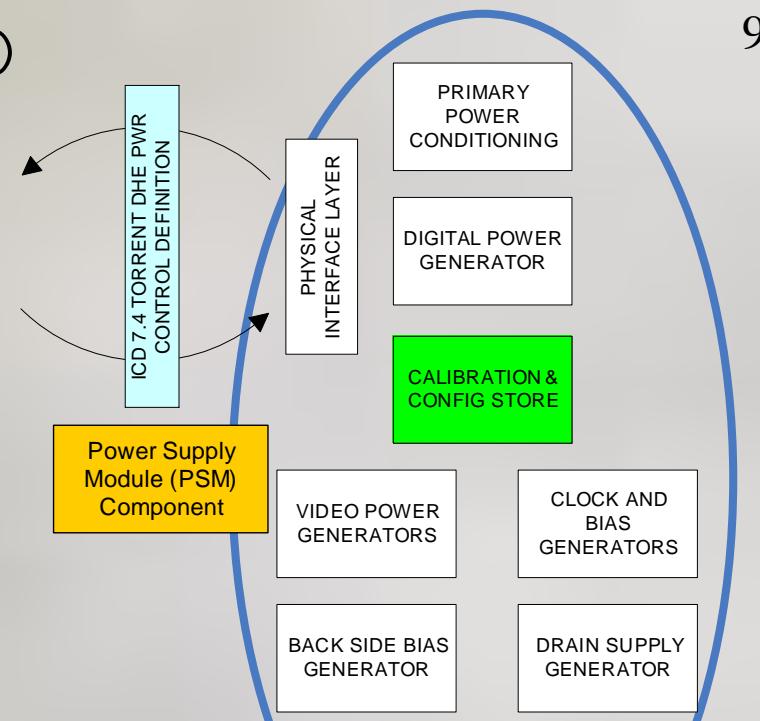


# Torrent Design

## Detector Head Electronics (DHE) System

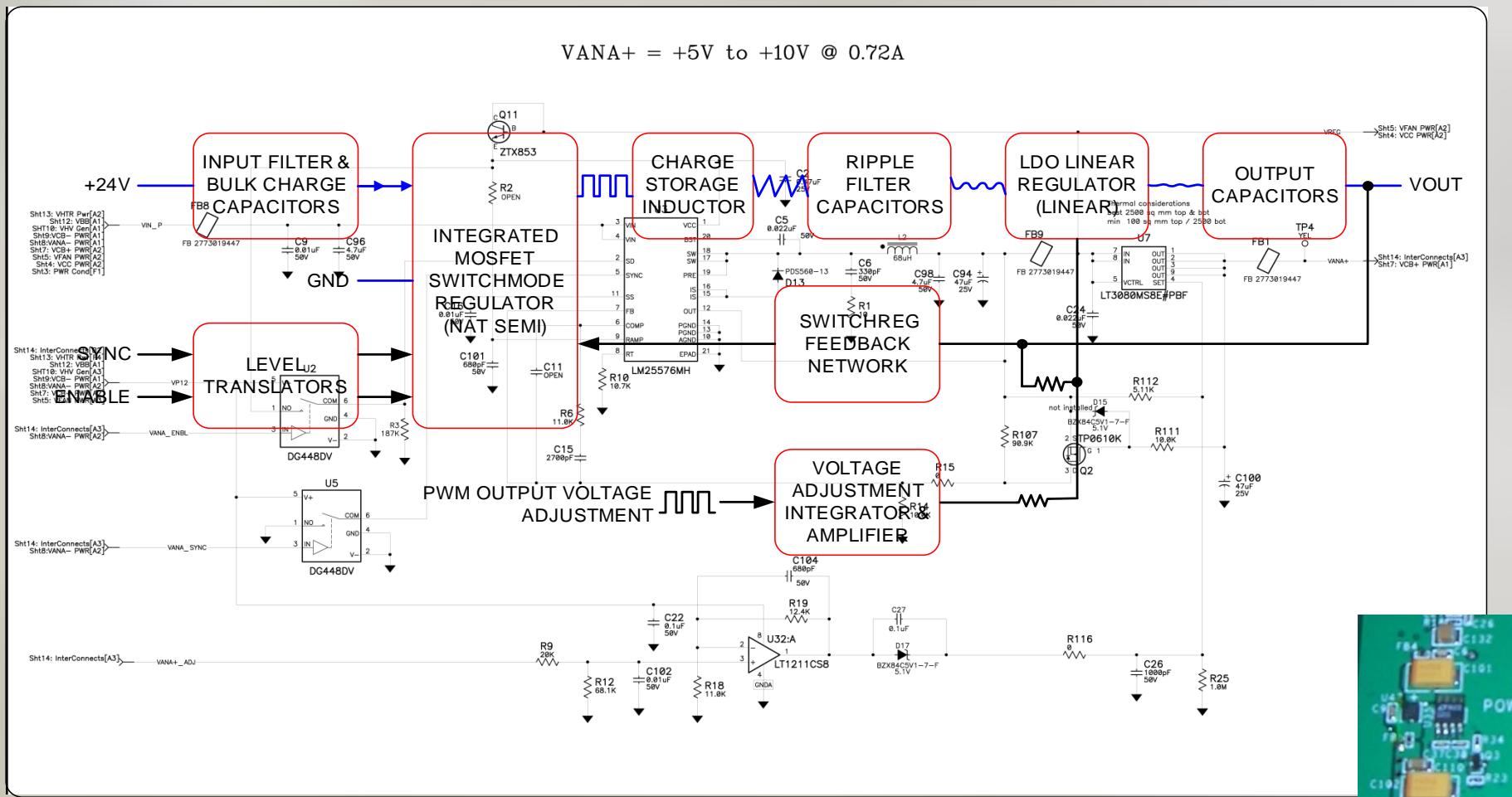


# Torrent Design – Power Supply Module (PSM)



| <u>Supply</u> | <u>In/Out</u> | <u>Voltage</u> | <u>I Nom (ma)</u> | <u>I max (ma)</u> | <u>Description</u>                      |                               |
|---------------|---------------|----------------|-------------------|-------------------|---|-------------------------------|
| VRAW          | INPUT         | 22 to 26       | 1000              | 2500              | Primary power input                     | DEWAR HEATER POWER CONTROL    |
| VCC           | OUTPUT        | +3.3           | 1130              | 3000              | Digital logic supply                    |                               |
| VFAN          | OUTPUT        | +7 to +14      | 300               | 400               | DHE temperature cor                     | PHYSICAL INTERFACE LAYER      |
| VANA+         | OUTPUT        | +5 to +10      | 400               | 720               | Video circuits +ve rail                 |                               |
| VANA-         | OUTPUT        | -5 to -10      | 250               | 720               | Video circuits -ve                      | ICD 7.6 PSM ⇄ TSM DEFINITIONS |
| VCB+          | OUTPUT        | +9 to +18      | 350               | 650               | Clock and low voltage bias circuits +ve |                               |
| VCB-          | OUTPUT        | -9 to -18      | 350               | 650               | Clock and low voltage bias circuits -ve |                               |
| VHV+          | OUTPUT        | +30 or +5      | 120               | 200               | High voltage bias circuits +ve          |                               |
| VHV-          | OUTPUT        | -30 or -5      | 120               | 200               | High voltage bias circuits -ve          |                               |
| VBB           | OUTPUT        | +/- 8 to 65    | 2                 | 10                | Back side bias supply                   |                               |
| VHTR          | OUTPUT        | 0 to 22        |                   | 500               | Detector temperature control            |                               |

# Torrent Design – PSM Switch Mode Regulators



- Conservative, efficient and common switch mode design
- Voltage adjustment using PWM signal
- Enable/disable capability
- Synchronization across 1 octave of frequency range
- Post regulation for DC precision and ripple rejection



# Torrent Design – PSM Synchronization and System Ground

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| f KHz | f x 2 | f x 3 | f x 4 | f x 6 | f x 8 |
|-------|-------|-------|-------|-------|-------|
| 70    |       | 210   |       | 420   |       |
| 80    | 160   | 240   |       | 480   |       |
| 90    | 180   |       |       | 540   | 720   |
| 100   | 200   | 300   |       | 600   | 800   |
| 110   | 220   | 330   |       | 660   | 880   |
| 120   | 240   | 360   |       | 720   | 960   |
| 125   | 250   | 375   |       | 750   | 1000  |
| 130   |       | 390   |       | 780   | 1040  |
| 140   |       | 420   |       | 840   | 1120  |
| 150   | 300   | 450   |       | 900   | 1280  |
| 160   | 320   |       |       | 960   | 1320  |
| 165   | 330   |       | 660   | 990   | 1360  |

| Supply  | Min KHz | Max KHz |
|---------|---------|---------|
| VCC     | 300     | 600     |
| +/-VANA | 660     | 1000    |
| +/-VHV  | 125     | 250     |
| Vlogic  | 750     | 2250    |

## Ripple Mitigation

Ripple  $\Delta V$  dependent on load and frequency.

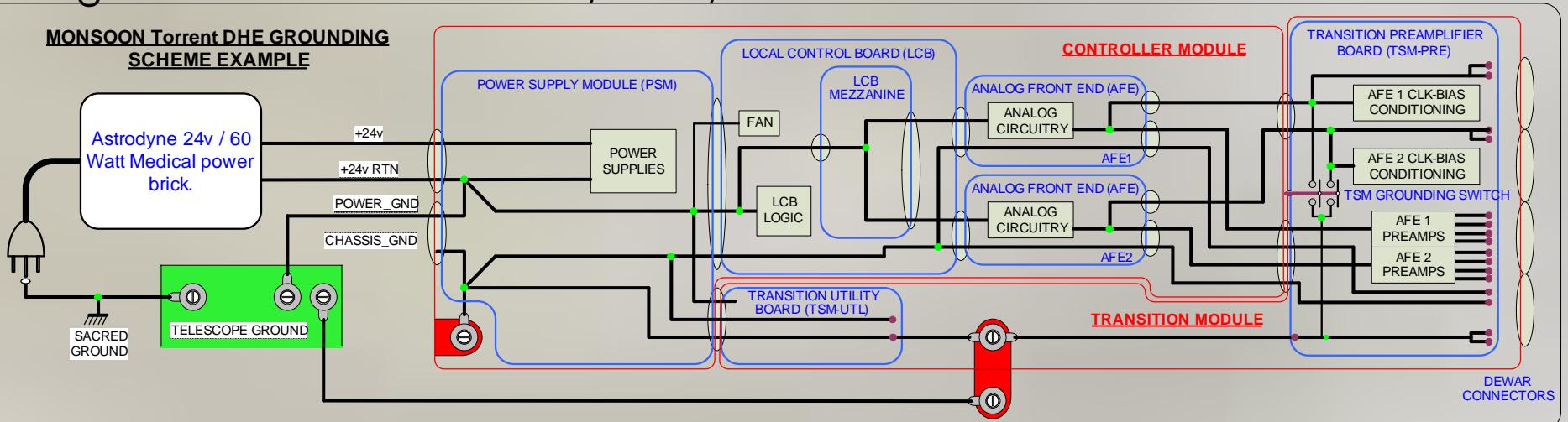
Constant load and freq.

Regulator and amplifier PSRR

Synchronous 'noise' is DC offset

Design Pixel Rate 50 — 500KPix/chan/sec

### MONSOON Torrent DHE GROUNDING SCHEME EXAMPLE





### Higher Efficiency

Less heat

Increased reliability

### Higher Frequency

Reduced size

Less weight

### Inherent Ripple Voltage

Synchronization makes this a DC offset on data

### High Frequency ‘spikes’

Controlled (slower) switching edges on sensitive supplies

At source filtering using ferrite magnetics

### Prototype PSM Performance

- ✓ Over 8 months of service. 2 failures. Both human error. Both repairable.
- ❑ Regulator voltage/current limits of synchronization and load met except +/- VHV load (70ma limit).
- ✓ xx% efficient. Low heat generation. Conductive heat transfer works.
- ✓ No detectable difference in noise levels between lab supply and PSM supply using shorted input tests.
- ✓ Power supply overcurrent, input over/under voltage protection works.

### Rev -A - Differences

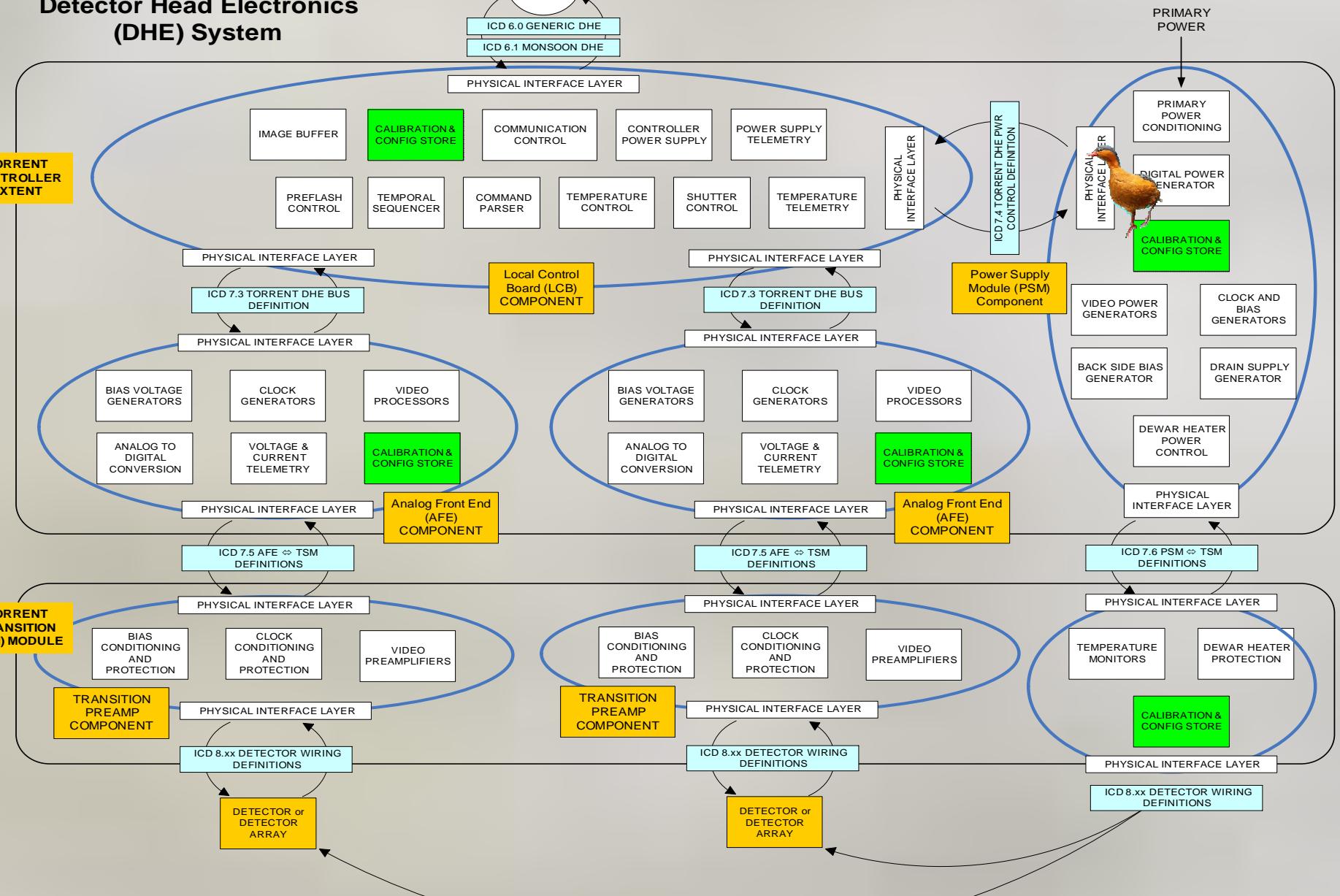
- Inclusion of the Vbb supply. Prototype tested.
- Redesign of VHV magnetics to meet 200ma limit
- Interdependence of power supplies removed – VANA & VHV.
- Problem on enables during power off fixed – change in enable polarity.

# Torrent Design –

# Calibration and Configuration

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## Detector Head Electronics (DHE) System

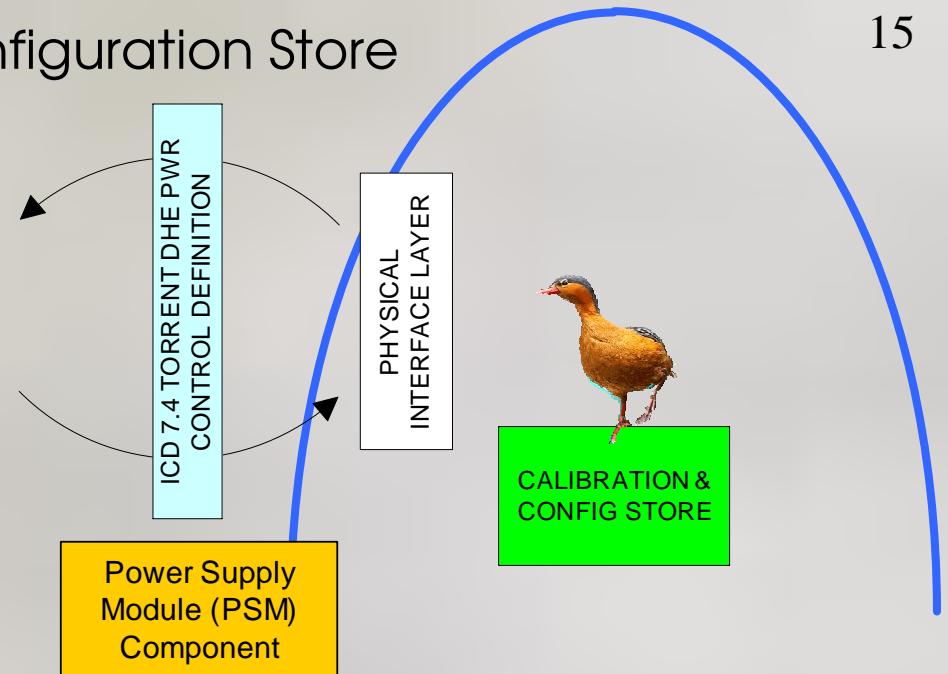


# Torrent Design – Calibration and Configuration Store

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## Function

- ✓ Store board calibration constants
- ✓ Supply unique hardware identifier
- ✓ Sense temperature of DHE boards



## Use

- Software builds dynamic DHE configuration at run time - Maintenance
- Software identifies detector system from Transition, carries safe limits
- Temperature telemetry for diagnostics

## Hardware

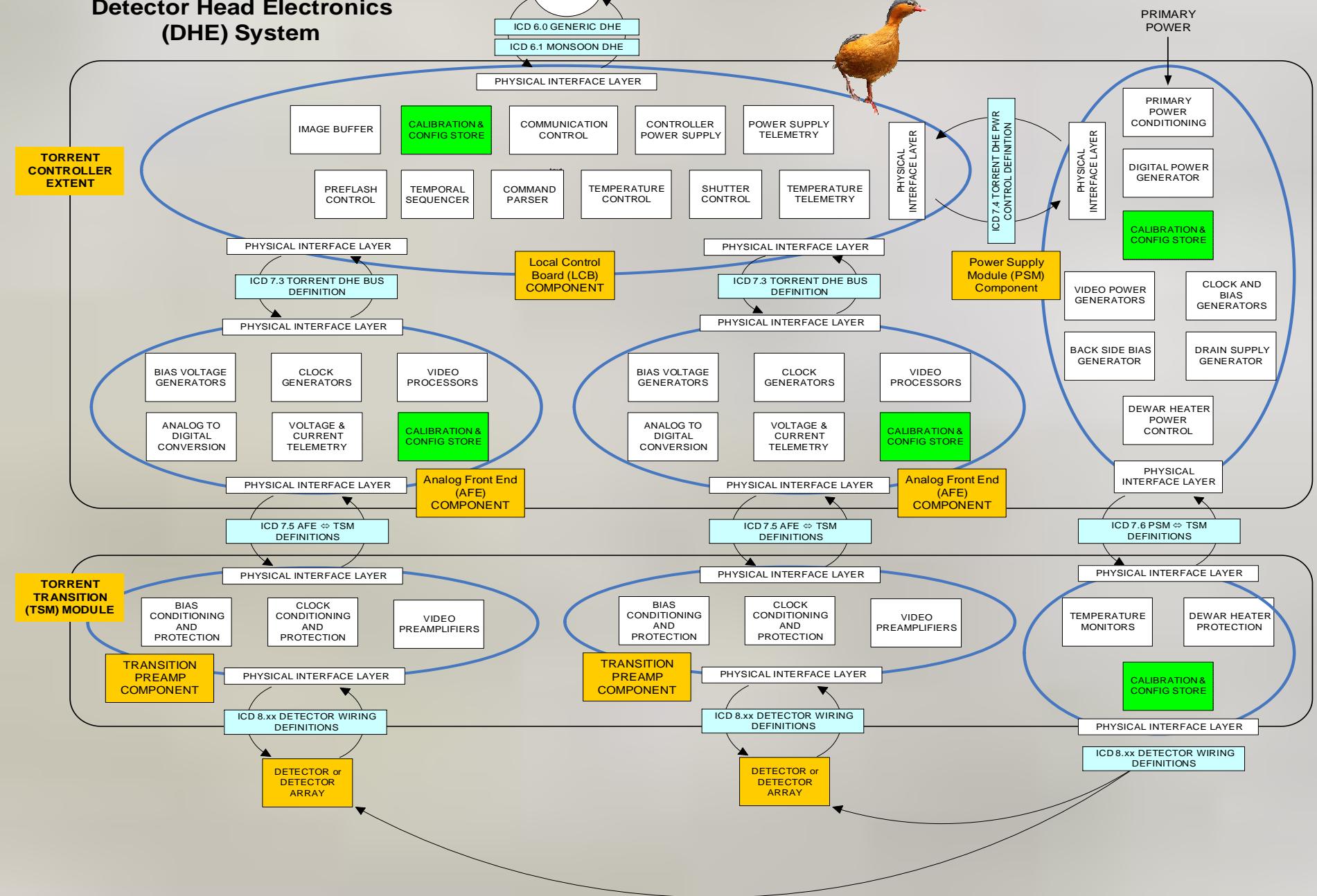
- Standard hardware circuit configuration for each DHE circuit board
- Uses I2C bus to test presence of board and to interrogate I2C devices
- isolated serial data line pull-up supply to prevent noise feed through

# Torrent Design

# Local Control Board (LCB)

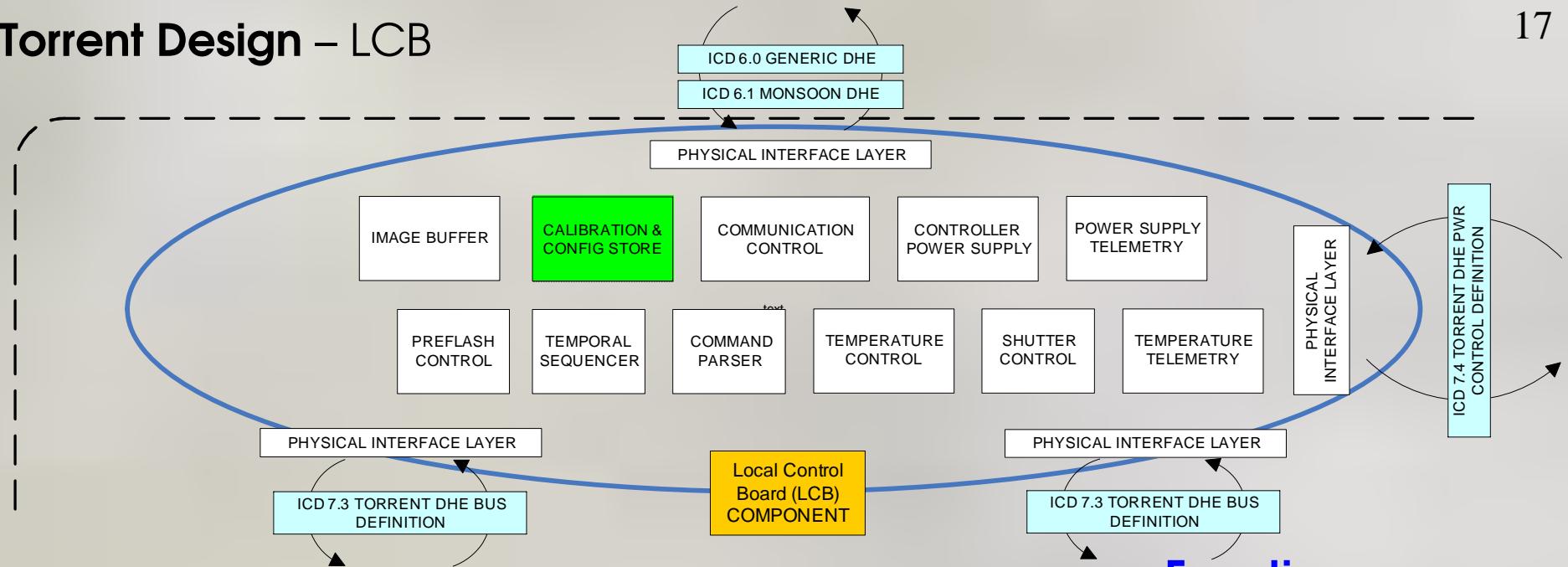
16

## Detector Head Electronics (DHE) System



# Torrent Design – LCB

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## Functions

Communications  
DHE Control  
Temporal Sequencing  
Image Buffering  
Telemetry  
PSM & Temp Servos

## Physical Interface Layer

- ✓ Optical Fiber – Systran SL100 – 1GBit/sec duplex – Fiberlink protocol
- ✓ Ethernet – GIGe option – 1Gbit/sec – GIGe protocol on IEEE 802.3
- ☐ High Speed Serial – 53MBit/sec – Via Sync port cables – Proprietary
- ✓ RS232 – 9600 baud – 3-wire debug and development port

## Command / Message formats

Optical Fiber – ICD 6.1 – 32-bit direct read/write to DHE address space

Ethernet – Command interpreter – 8-bit ASCII wrapped version of ICD 6.1

RS232 – Command interpreter – 8-bit ASCII wrapped version of ICD 6.1

- Command stream echo disable capability via command attribute
- Command / Message copy to any comms port via software attribute
- Pixel data routing through any comm port

256 Mbytes 2-port dynamic memory designed to support pixel data FIFO mode or full image buffering mode

Organized as 128M x 16-bit words or 64M x 32-bit words depending on detector mode (NIR or CCD)

Capacity to buffer a 2Kx2K NIR array for a complete pre/post integration cycle using 16 Fowler reads and 32 digital averages

Capacity to buffer an 8Kx8K CCD mosaic in 18-bit data format

- Pixel data descrambling in full image buffer mode
- Pixel statistics logged during readout – available as attributes
- Frame and Line strobes available for GIIGe and Systran data streams
- Power down available if stream mode employed
- 18-bit or scaled 16-bit data format
- Data path accommodates 80MPix/sec (limited by communication path to 25MPix/sec)



Implements ICD 6.1 with four commands:

Read 32-bit value – as a variable by attribute name

Write 32-bit value – As a variable or as a function trigger by attribute

Asynchronous command – Used to synchronize DHE to PAN

Start Exposure command – with 8-bit start vector to sequencer.

- ✓ Emulates MONSOON Orange protocol
- ✓ Multi-user – commands / messages through any comms port
- ✓ Echo acknowledgement to commands
- ✓ Internal bus uses six ‘module’ addresses instead of eight slot addresses  
(LCB, PSM, CFG, PIX, AFE, CLK) with fixed address assignment
- ✓ Automated extraction of DHE register space via VHDL source code  
comments field

✓ Emulates MONSOON Orange MCB sequencer

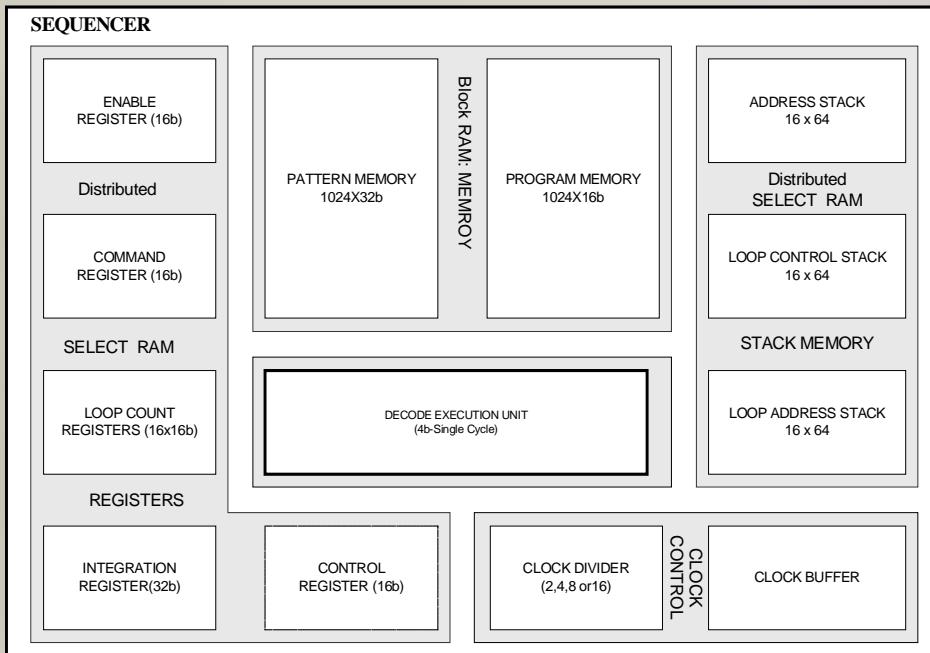
Orange assembler code usable but requires:

Module address space used instead of Slot Address

Timebase change for DSC command (38ns Torrent vs 50ns Orange)

New assembler (Tasm) to account for 32-bit word space

Orange micro-sequencer for CDS functions not needed



- ✓ Implements ICD 7.3 and 7.4 for CCD and NIR AFE boards

Describes complete signal groups and interface mechanisms

All digital interface, synchronous to one clock source (80 MHz)

Separate power supply system for AFEs – no signal return path mixing

Minimal digital logic on AFE – only signal latches

Digital noise barrier using voltage translators and intermediate interface voltage supply

Allows separate or ganged control of multiple AFE boards

- ✓ Flexible interface configured entirely by firmware
- ✓ All signals are input/output/bi-directional capable (> 160 I/O circuits)
- ✓ Controlled delay characteristics for LCB input data signals



See <http://www.noao.edu/ets/monsoon/ICD.html>

## LCB board – Digital functions

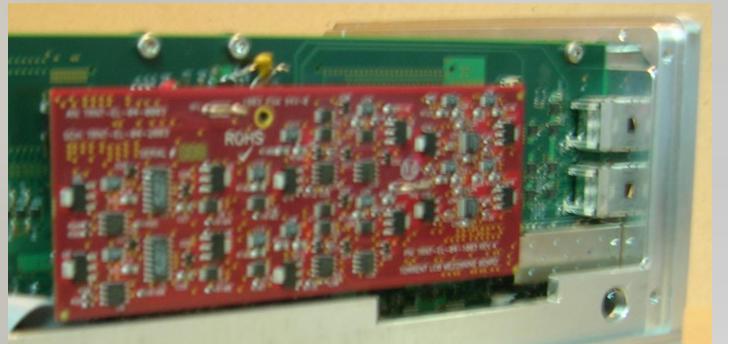
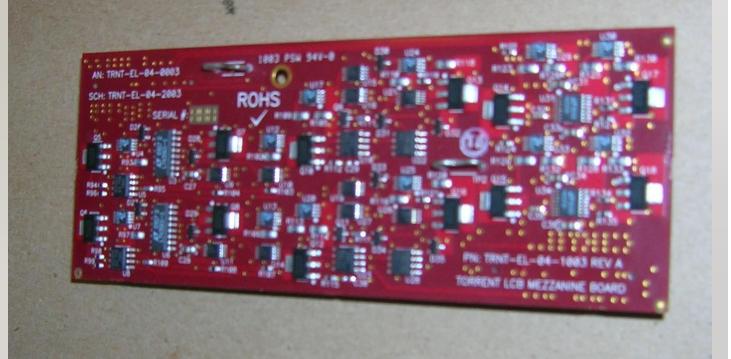
- ✓ Individual enable/disable of AFE power supply potentials
- ✓ Controls AFE power on with sequenced delays and status check

## LCB-MEZ board – Analog functions

Plugs directly into LCB as a mezzanine board

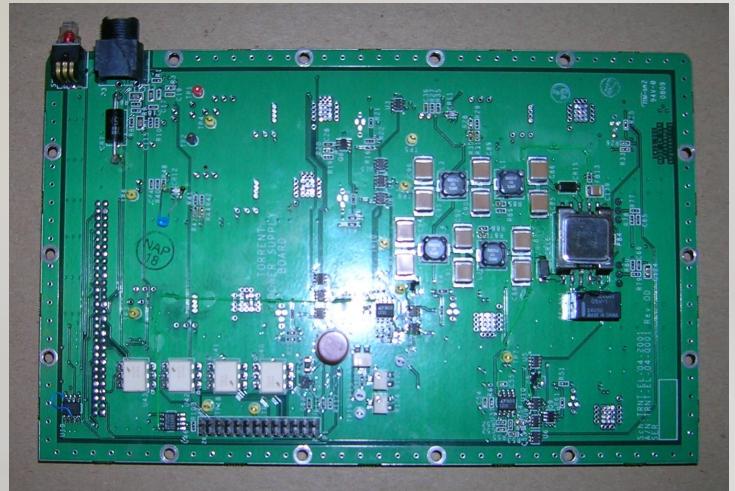
- ✓ Provides separation of digital and analog grounds back to the PSM
- ✓ Provides current telemetry for each AFE board supply
- ✓ Provides hardware under voltage and over current protection
- ✓ Provides supply status for safeguarding

DHE and detector



## Control of Power Supply Module (PSM)

- ✓ PSM detector high voltage polarity
- ✓ PSM analog supply enables
- ✓ PSM analog voltage adjustment
- ✓ PSM Synchronization to pixel rate
- ✓ Reads PSM voltage telemetry
- Servos PSM analog voltages to eliminate temperature drift and load variance
- ✓ DHE temperature control servo for fan supply regulator (DHE temperature stabilization)
- Detector temperature control servo for detector heater current supply



### Detector Voltage Telemetry

Scanned every 200ms (adjustable / allows disable during read)

- ✓ Bias and clock voltages
- ✓ AFE circuit reference and supply voltages

### DHE Telemetry

Fixed scan rate

- ✓ Integration status - Shutter status, Integration time remaining, etc.
- ✓ Temperatures – DHE, Boards, Detector, heater power, etc.
- ✓ Power supply status – Power good, Power active
- ✓ AFE power supply voltages
- ✓ AFE power supply currents

➤ Available as read-only attributes

➤ Calibration values for engineering units carried on each board

### Prototype LCB Performance

- ✓ All communications proved – nonexistent transmission errors
- ✓ Pixel data path proved – no loss of data observed in 5 months
- ✓ DHE Control structure proven on all firmware modules
- ✓ Sequencer tested and verified
- ✓ AFE Power control operational – fault modes verified
- ❑ Power supply control working – small amount of ripple on servos

### Work to be done

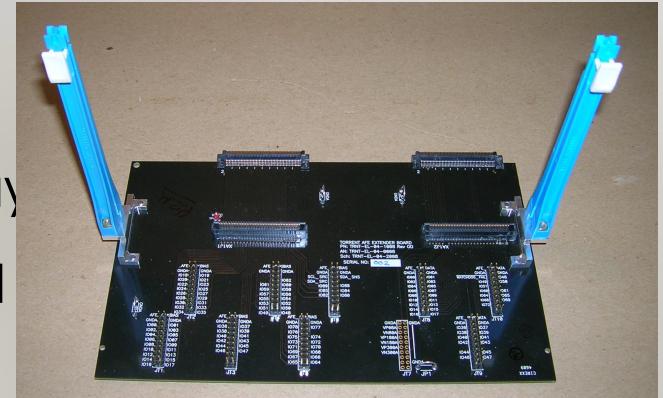
- Hardware respin required to correct: clock generator filter, GIGe ↔ LCB interface connector, memory power supply problem, etc.
- Firmware work required for: synch port comms and sync port timing calibration, power supply servo ripple, Image buffer memory descrambler.
- Firmware documentation to be written

## Front Line Tools

- ❑ Software filters (checkState)
- ✓ Engineering console: full access to attributes (controlled access)
- ✓ Two indicators for DHE operational state on external panel
- ✓ Power condition indicator
- ? Controller exchange at detector cryostat using generic module
- ❑ Full documentation available

## Second tier Tools

- ? Common module spares – plug and play
- ✓ Extender board for access to AFE board
- ✓ Debug comms port – always available
- ✓ Multiplexed debug port for firmware support – Test ports for AFE
- ❑ Board & Controller functional test HW and SW available
- ❑ Documented module / board histories





Stay Awake !!

Next Up:

AFE / TSM Description

Mark Hunten

